A HARDWARE AND SOFTWARE INTEGRATED POWER OPTIMIZATION APPROACH WITH POWER AWARE SIMULATIONS AT SOC

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INTRODUCTION

A systematic approach is inculcated to target an efficient and smooth verification flow for low-power simulations for large SOCs.
Analysis of power/voltage/clock domains ➔ Defining verification scope
One time compile ➔ Loading the power information of design
PMIC controller ➔ Mimic the behavior in the test bench
Power operations isolation, level shifters, retention ➔ Checkers to reinforce

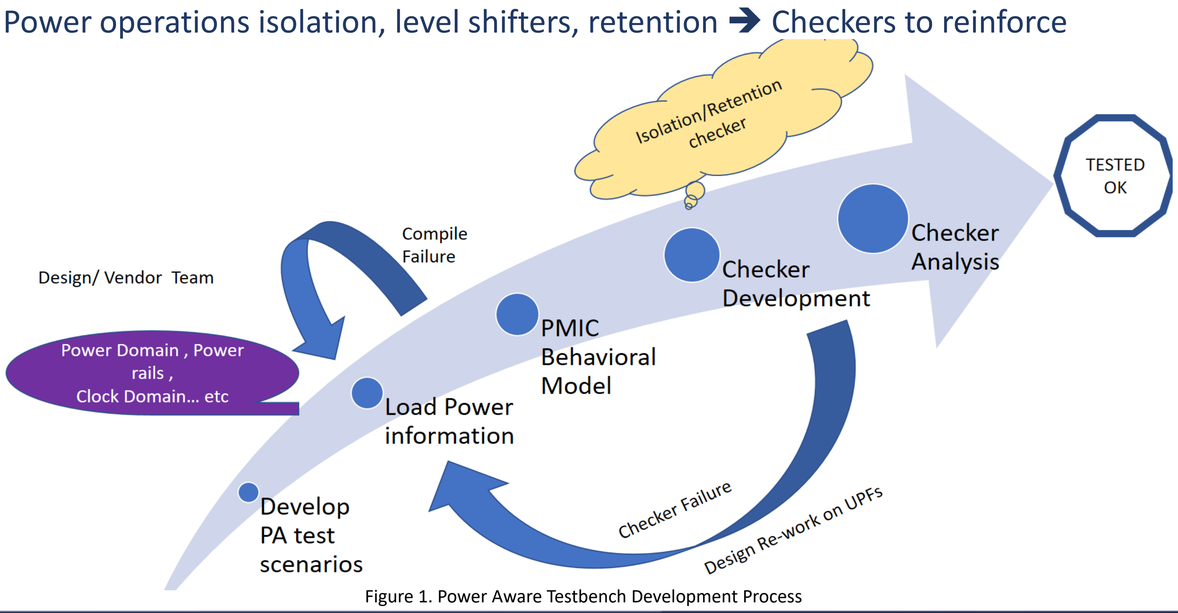
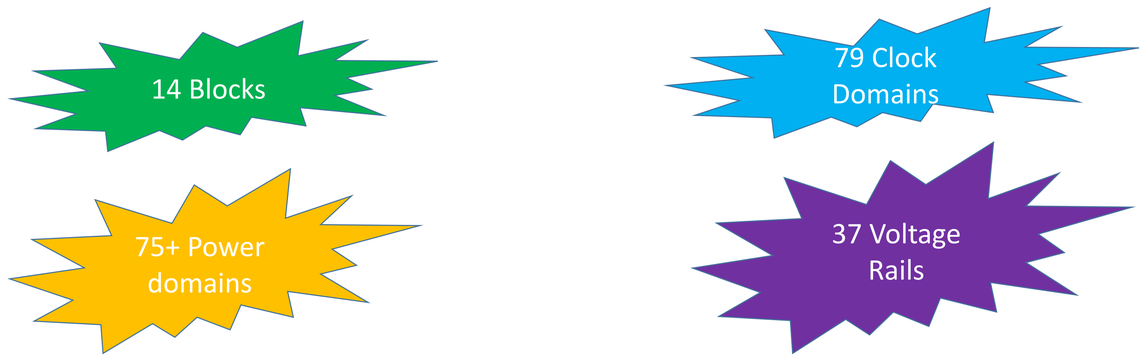


Figure 1. Power Aware Testbench Development Process

PROPOSED METHODOLOGY



- Variable voltage level ➔ Operating from 0.6V to 3.3V.
- Switchable power supplies ➔ Power gating
- Clock shut off ➔ Clock gating when PD is idle.
- Isolation cells ➔ Avoid leakage to nearby PDs.
- Level shifters ➔ Sampling signals that cross voltage levels.
- Retention ➔ Data saved during power shut off and restored during power on

POWER CONTROLLER ACHITECTURE AND POWER STATES

Figure 3. Power Down Flow

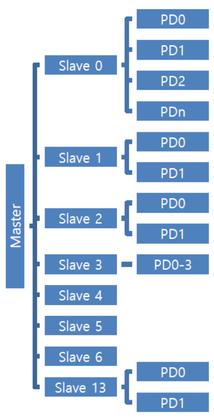


Figure 4. Master Slave Architecture

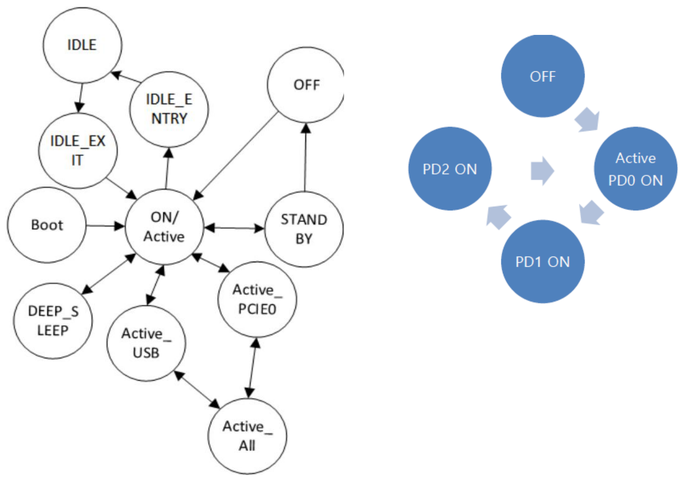


Figure 5. Slave Power Transitions

POWER ESTIMATION PROCESS

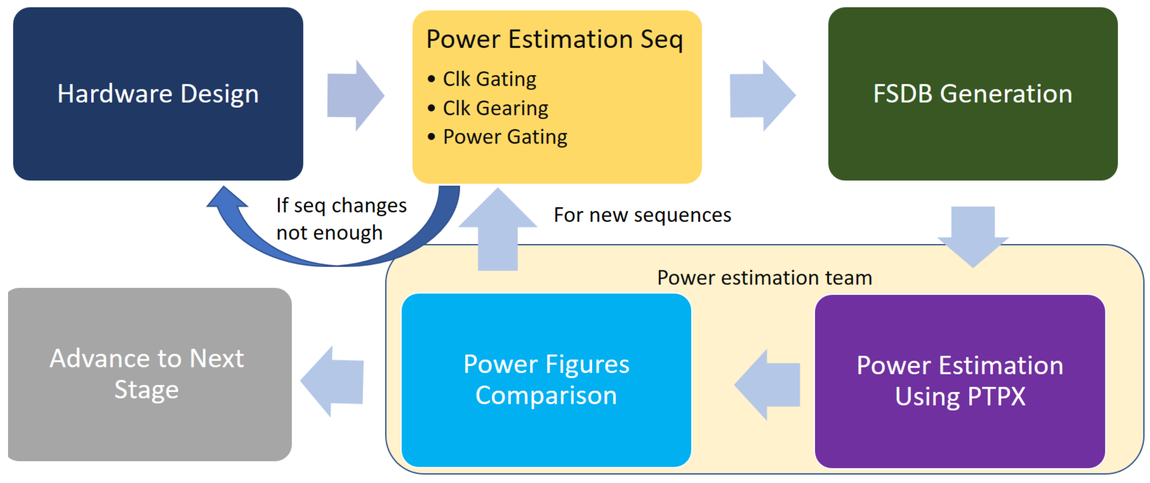
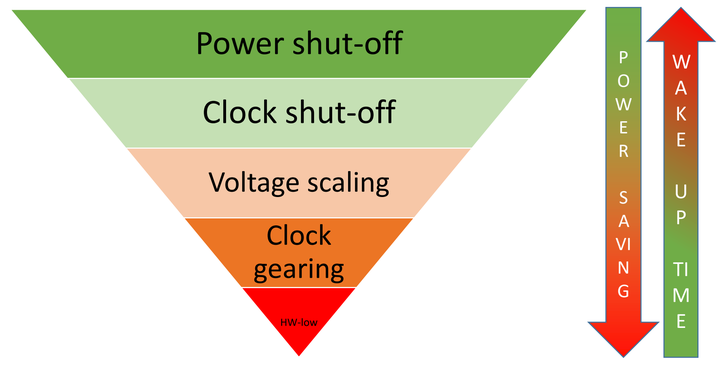


Figure 2. Power Estimation Process

Power Estimation Done At :
- RTL Simulation
- Power Aware RTL Simulation
- GLS Simulation
- Power Aware GLS simulation

RESULT

- ✓ Optimized process of HW & SW based approach
- ✓ Developed Intermediate Power States – Lower consumption & Faster Wakeup
- ✓ Power Rail off scenario for Power estimation



Power Gating(PG)/Clock Gating(CG) from testcase analysis at SOC Level						
		HW Controlled	SW Controlled			
Scenario	Low Power Stages	Master PG	Block PG	Master CG	IP CG	% Power Saved
A	Level0					0%
B	Level1				Yes	42%
C	Level2		Yes			68%
D	Level3			Yes		52%
E	Level4	Yes	Yes			83%

Table1. Chip level power scenarios and power savings

LEAK POWER	IDLE POWER	POWER GATED IDLE
40mW	5.99mW	0.58mW

Table 2. Power figures at block level

	Block Level Analysis						
Scenario	System Register, NOC	MCU	Camera controller	Image Processor	Display controller	DMA	Power Saving
A	FC, NOP (100Mhz)	FC,NOP (800Mhz)	FC,NOP(800 Mhz)	FC,NOP(800Mhz)	FC,NOP (800Mhz)	FC,NOP (800Mhz)	0%
B	FC, NOP (100Mhz)	FC,NOP (800Mhz)	Clock gearing(100Mhz)	Clock gearing(100Mhz)	Clock gearing(100Mhz)	Clock gearing(100Mhz)	10%
C	FC, NOP (100Mhz)	FC,NOP (800Mhz)	FC,NOP (800Mhz)	FC,NOP (800Mhz)	Clock Gating	FC,NOP (800Mhz)	25%
D	FC, NOP (100Mhz)	FC,NOP (800Mhz)	Clock Gating	Clock gating	Clock Gating	Clock Gating	40%
E	FC, NOP (100Mhz)	Clock Gearing(100Mhz)	Clock Gating	Clock gating	Power Gating	Clock Gating	58%
F	FC, NOP (100Mhz)	FC,NOP (800Mhz)	Power Gating	Power Gating	Power Gating	Power Gating	68%
G	FC, NOP (100Mhz)	Clock Gated	Power Gating	Power Gating	Power Gating	Power Gating	79%
H	Clock Gated	Power Gated	Power Gating	Power Gating	Power Gating	Power Gating	91%

Table 3. Power saving in Block level Power down states/ Scenarios

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