Variation-Aware Modeling Method for MRAM Behavior Model using System-Verilog

S. Do, S. Shin, J. Jang, D. Kim
Samsung Electronics, Foundry Division
1-1, Samsungjeonja-ro, Hwaseong-si,
Gyeonggi-do, Korea, 18448

***Abstract*-IP verification is an essential process while designing IP. It has become more significant with the increased demand for silicon in automobiles. IP verification includes verifying logical operations, which runs logical simulations and requires behavioral models written in Verilog or VHDL. Behavioral models are essential for small size gate to large memories. For small-sized circuits such as gates and standard cells, it is easy to implement all operations. However, large-sized IPs such as memory usually reflect only key operations because it is impossible to implement all the detailed operations and consider physical characteristics. In addition, in conventional modeling methods, some specialized devices, such as MTJ devices for MRAM, having unique random characteristics cannot be supported. In this paper, we introduce memory bit-cell modeling method, which enables various test operation for embedded MRAM. The proposed modeling methods are implemented for solid IP validation and it supports not only the MRAM but also various types of memories.**

I. Introduction

In general, behavioral models are not more complex than circuits or physical layouts because they reflect only the logical operations of IP. For example, In the case of SRAM, the bit cell in which the data is recorded is simply represented as a register in High Definition Language (HDL). Similar to the demand for IP validation, demand for behavioral model has also increased. Normally, various verification methods are being studied to increase the integrity of the behavioral model. However, from the IP validation perspective, it is as important to enhance the behavioral model itself as to verify the behavioral model, because the model that's modeled in detail support IP verification scenario before fabrication. In this paper, we introduce memory bit-cell modeling method for an MRAM behavior model using a System-Verilog. Our modeling method supports solid verification and reflects Write-time variation and Write-voltage variation.

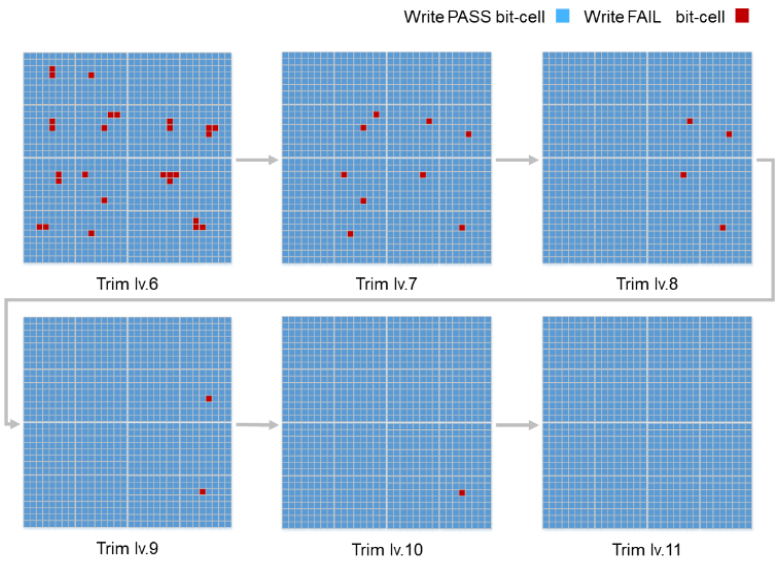

Fig. 1. Bit-cell array variation aware simulation illustration

II. Related Work

Behavioral models are essential for system-level logical simulation. The behavioral model simplifies the complex behavior of individual IPs and enables logical simulation. For simple circuits such as standard cell, modeling is easier in most of the cases. However, for big circuits such as memory, it is almost impossible to implement all analog circuit base operation into the behavior model. Therefore, most memory behavior model only implement important main functions, such as read, write, scan shift, and capture. As the importance of chip verification increases, the need to implement test functions also increases. Many studies, including us, have tried to model complex test functions. Some of them use Verilog-A to model the Programmable Metallization Cell (PMC), which is a non-volatile memory device that generates oxide through ion flow and uses this behavior model to adjust the electrical resistance value to store data in the cell as similar with MRAM MTJ. [1].This prior work modeled the operation of the PMC cell using Verilog-A based on the previously measured I-V characteristics of the PMC cell. However, Verilog-A modeling is more complicated and time-consuming than digital modeling such as Verilog or System-Verilog. Considering the reasons for the existence of behavioral models, it is clear that modeling with Verilog or System-Verilog is most desirable.

In addition, other previous studies [2] have modeled analog operations such as PLL with high accuracy and System-Verilog alone. PLL circuit is used for clock generation, clock and data recovery, and high-speed I/Os. In this case, the analog operations of the PLL, such as PLL locking behavior, jitter, and phase noise were modeled using System-Verilog, that are used for pre-silicon digital verification. Because the System-Verilog modeling methodology provides more data types and higher abstraction than Verilog-A, more accurate and flexible models could be implemented. Specifically, Verilog-A is a language used for analog simulation. With PLL characteristics that require consideration of both digital and analog operations, it is advantageous to use System-Verilog rather than Verilog-A.

III. MRAM Behavior And Modeling

Most memory operations can be simply implemented with a behavior model. This is because from an operational point of view, writing and reading in memory is a simple operation of storing and reading data, and in the case of SRAM in which bit-cell is implemented as a set of transistors, this is expressed as a register in behavior modeling. However, MRAM, an emerging memory of a non-volatile memory, has a unique random characteristic of Magnetic Tunnel Junction (MTJ) bit-cell device. To run the internal test operation for MTJ devices, conventional modeling method could not support. The following sections introduces the modeling method of MRAM behavior model.

A. MTJ Background

MTJ has a structure with two magnetic layers separated by an insulating barrier layer. The tunneling current flowing through the MTJ is determined by the thickness of the tunneling barrier and the voltage applied to both ends. The determined tunneling current may change the magnetization direction of the magnetic material at both ends. In addition, the magnetoresistance of MTJ changes according to the combination of magnetic layer directions [3]. MTJs with these characteristics are the main devices used in MRAM bit cells as illustrated in Fig. 2. However, reliability and endurance issues occur with the higher voltages [4]. Accordingly, the MRAM trims the write voltage to find and use the optimal write voltage according to the process change.

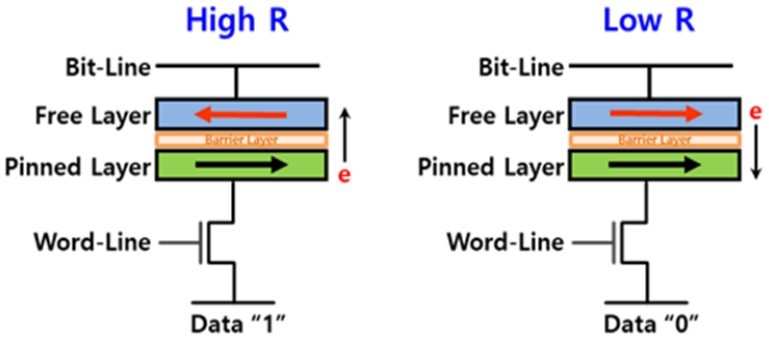

Fig. 2. Data record methodology of MTJ device

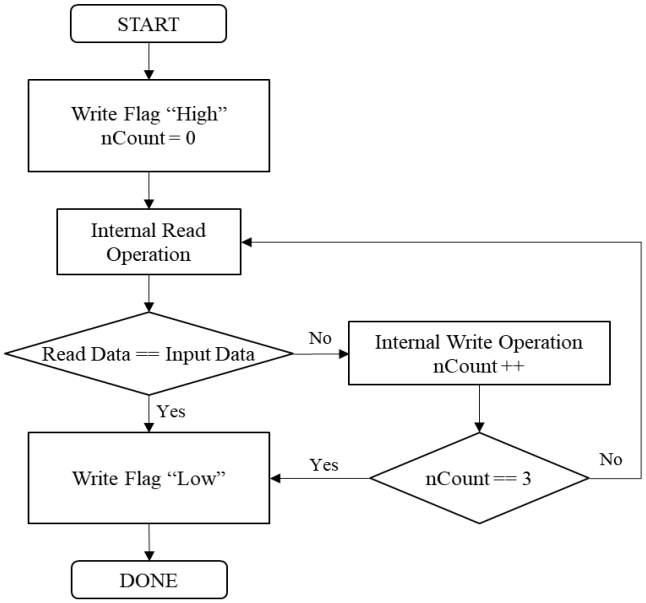

Fig. 3. Write operation flow chart of MRAM

B. MRAM write operation

For an existing memory-write operation, write-0 or write-1 is only a single operation. Because a single write operation can ensure data writing. However, due to the probabilistic write characteristics of the MRAM MTJ device, a single write operation cannot ensure data write. To overcome these probabilistic write characteristics, the MRAM of the Samsung Foundry has multiple internal write and read operations in a single write operation. This internal write operation has probabilities. Using multiple internal write operations, the memory achieves an almost 100% write probability and the internal read operation ensures a write operation. In addition, using the write verify scheme with write flag, MRAM notifies the write completion status. However, due to this multi-probabilistic internal write operation, the write time, rather than the conventional SRAM, is variable. In addition to time variation, MRAM has a write voltage variation also. Since MRAM is a resistive memory, the MTJ write voltage characteristic also has a variation following the process variation. Fig. 3-4 illustrates our MRAM-write operation.

C. Modeling Method

In memory bit-cell modeling method, we use two different modeling approach: Time variation and voltage variation. As the probabilistic write operation of MTJ bit-cell in MRAM, data write time might vary for each write cycle. That is, the write voltage characteristic also has a variation according to the process variation. Following sections describes each modeling method using various sample Verilog code.

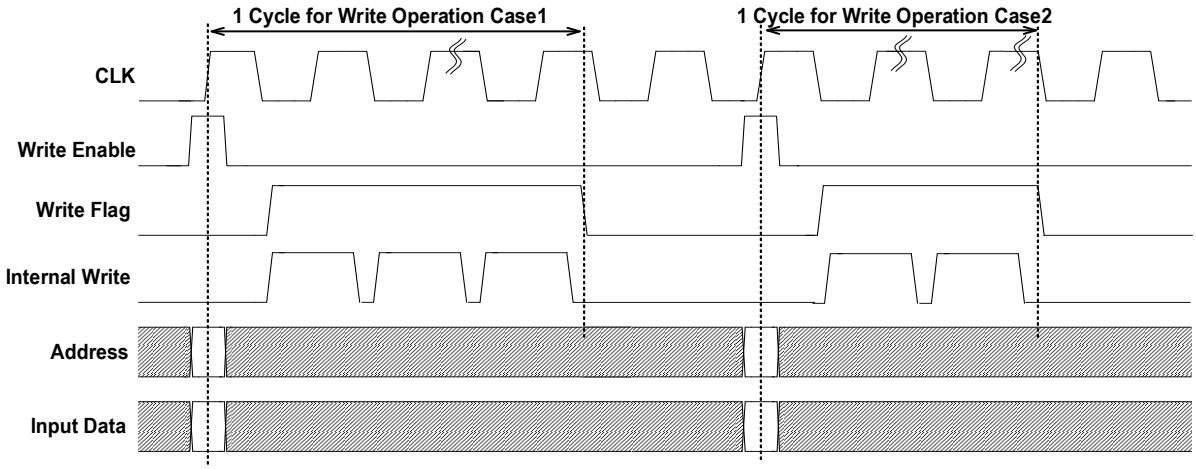

Fig. 4. Write operation timing diagram of MRAM

```
`ifdef TIMING_VARIATION
  reg [6:0] random_seed;
  always @(negedge CK) begin;
    random_seed = $urandom_range(0,100);
    if ( WRITE_BUSY === 1 ) begin
      if ( random_seed < ("probability") ) begin
        disable WRITE_BISY;
        WRITE_DONE;
      end
    end
  endl=
`endif
```

Fig. 5. Abstract timing variation modeling

```
// Memory definition
reg [(word_width)*mux-1:0] mem[0:num_rows-1];
reg [(word_width)*mux-1:0] mem0[0:num_repair_rows-1];
reg [(word_width)*mux-1:0] mem1[0:num_repair_rows-1];
reg [(word_width)*mux-1:0] mem2[0:num_repair_rows-1];
reg [(word_width)*mux-1:0] mem3[0:num_repair_rows-1];
reg [(word_width)*mux-1:0] mem4[0:num_repair_rows-1];
reg [(word_width)*mux-1:0] mem5[0:num_repair_rows-1];
reg [(word_width)*mux-1:0] mem6[0:num_repair_rows-1];
reg [(word_width)*mux-1:0] mem7[0:num_repair_rows-1];
```

Fig. 6. Conventional memory register

1) Time-Variation Modeling

In this modeling method, a random write time mode is added to the MRAM behavior model using a random internal write operation with the actual write operation of the circuit. Using the *$urandom_range* System-Verilog system task, individual internal write operations allow users to define write probabilities. Based on probability, each internal write sequence could continue or stop internal write sequence as illustrated in Fig. 5. This random function generates all possible write time variation, and keep proceed the internal write operation to achieve proper write operation. However, writing operations in behavioral models must eventually be ensured. Thus, when the write time reaches the limit of the specified write time, the write operation occurs. From this mechanism, the write time fluctuates and ensures proper write operation within the specification.

2) Voltage-Variation Modeling

In this modeling method, the change in write voltage is caused by the process variation. Because this variation data is occurred during fabrication, appropriate variation characteristics must be obtained from the process engineer to model the voltage variation. Table 1 describes fail bit calculation based on voltage variation data provided from the process engineer. From the silicon-based write voltage characteristic, we can model the write voltage recognition operation using the System-Verilog language. We generate individual minimum required write voltages for all bit cells of the MRAM and use that voltage information while writing data for the bit cells. Since the write voltage characteristic of the MTJ bit-cell follows a normal distribution, we use *$dist_normal* System-Verilog task to generate the minimum required voltage for the bit-cell. In addition, to store the individual minimum required voltages for each bit cell, a typedef syntax is used to create a user-defined data_type called mbit. Fig. 6 illustrates the conventional memory define and Fig. 7 illustrates our proposed memory define, which can contain the reference voltage value.

```
// mbit definition
typedef struct packed {
  logic data;
  bit [9:0] ref1_voltage;
  bit [9:0] ref0_voltage;
} mbit;
// New Memory definition
mbit [(word_width)*mux-1:0] mem[0:num_rows-1];
mbit [(word_width)*mux-1:0] mem0[0:num_repair_rows-1];
mbit [(word_width)*mux-1:0] mem1[0:num_repair_rows-1];
mbit [(word_width)*mux-1:0] mem2[0:num_repair_rows-1];
mbit [(word_width)*mux-1:0] mem3[0:num_repair_rows-1];
mbit [(word_width)*mux-1:0] mem4[0:num_repair_rows-1];
mbit [(word_width)*mux-1:0] mem5[0:num_repair_rows-1];
mbit [(word_width)*mux-1:0] mem6[0:num_repair_rows-1];
mbit [(word_width)*mux-1:0] mem7[0:num_repair_rows-1];
```

Fig. 7. New data type for memory register

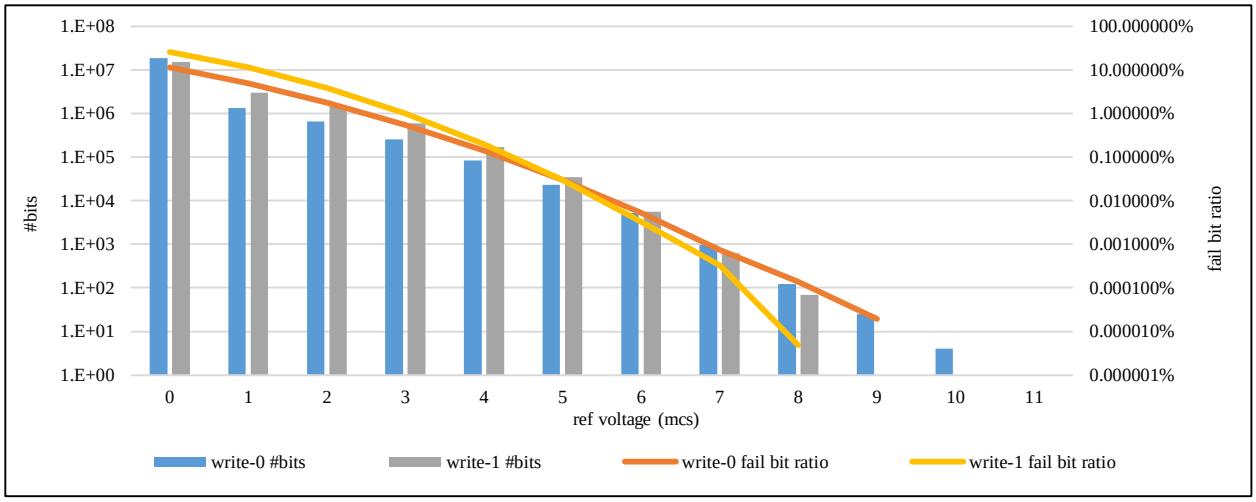

Fig. 8. 16 Mb MRAM Write reference voltage profile

IV. Simulation Result

The main purpose of this model is to use variation-aware test operation while verifying Digital Nonvolatile-memory Assist (DNA) IP operation for embedded MRAM. Fig. 9 illustrates conventional fixed write time simulation result with signal diagram with Verilog simulator. As the write time is fixed, write busy flag (WBF) signal rise and fall in regular while sequential writing. As illustrated in Fig. 10, time variation operation, Verilog model allows write time variations in random write time mode.

In addition, using the voltage variation mode, an intended write failure operation for a bit cell that does not satisfy the required minimum write voltage may be viewed. It can also be seen that write failure bits increase or decrease in terms of test pin settings by trimming the reference write voltage using the test pin. Fig 8. and Table I represent the fail-bit number and ratio of embedded MRAM in terms of write voltage trimming. Originally, this variation data was provided as voltage value from the process engineer. However, due to security issues, it has been replaced with a trimming value for the model, not an actual value. This variation-aware model operation is verified with DNA IP which controls this MRAM for IP validation. Furthermore, this voltage-aware write operation also cross-checked with Siemens TMBIST solution under development to support MRAM in the future.

TABLE I
TRIM-VALUE WITH FAILURE BIT-CELL COUNT (WRITE-0 CASE / WRITE-1 CASE)

Write-0		FAIL Ratio	Failure bit-cell # (ideal)		Write-1		FAIL Ratio	Failure bit-cell # (ideal)	
MCS[38:35]	MCS[34]		16 Mb	128 Mb	MCS[33:30]	MCS[29]		16 Mb	128 Mb
0	High	21.83500%	3,663,305	29,306,443	0	High	45.57641%	7,646,453	61,171,625
1		11.08118%	1,859,114	14,872,908	1		25.24925%	4,236,122	33,888,975
2		4.77904%	801,789	6,414,313	2		11.08118%	1,859,114	14,872,908
3		1.73814%	291,611	2,332,890	3		3.77202%	632,840	5,062,717
4		0.53009%	88,935	711,478	4		0.98153%	164,674	1,317,391
5		0.13499%	22,648	181,180	5		0.19330%	32,431	259,447
6		0.02861%	4,800	38,402	6		0.02861%	4,800	38,402
7		0.00504%	845	6,758	7		0.00317%	531	4,251
8		0.00073%	123	986	8		0.00026%	44	351
9		0.00009%	15	119	9		0.00002%	3	21
10		0.00001%	1	12	10		0.00000%	0	1
11		0.00000%	0	1	11		0.00000%	0	0
12		0.00000%	0	0	12		0.00000%	0	0
13		0.00000%	0	0	13		0.00000%	0	0
14		0.00000%	0	0	14		0.00000%	0	0
15		0.00000%	0	0	15		0.00000%	0	0

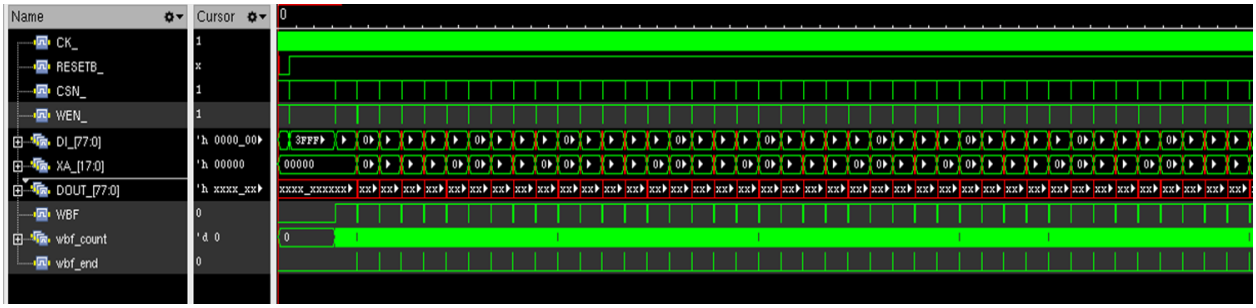

Fig. 10. Fixed time write operation simulation result

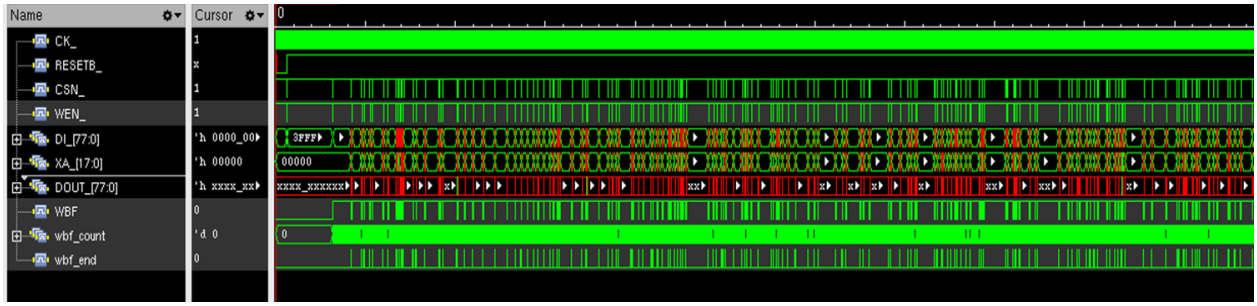

Fig. 9. Time variation write operation simulation result

V. Conclusion

IP verification is essential to achieve the reliability of the Foundry library from the perspective of the Foundry business. In addition, the importance of such verification is higher for basic IPs such as embedded memory. While it is almost impossible to implement all actions for the behavior model, modeling as many operations as possible is good for robust IP verification. To improve the reliability of the underlying IP of Samsung Foundry, we implement variation-aware testing method using the System-Verilog language in the behavior model. The behavioral model we developed supports variation-aware operations while testing and preventing avoidable human errors. In addition, the modeling method we proposed can be extended to various types of memory IPs written in the system-Verilog language.

Furthermore, our proposal utilized not only circuit characteristic modeling but also real process data values of MRAM bit-cell characteristics and applied them to the behavioral model. Through this, various test functions, trimming, and calibration characteristics required for verifying MRAM, a complex memory, were implemented, making it possible to perform more precise pre-silicon digital verification than before.

Acknowledgment

We would like to express our deepest gratitude to our team leader EVP Seiseung Yoon, project leader Jonghoon Jung, and part leader Dongho Shin for their support on this project. Also, we thank Bharath Shankar and Biswajit Behera for their excellent language correction.

References

[1] D. A. Dimplu and F. Wang, "Behavior Modeling of Programmable Metallization Cell Using Verilog-A," 2012 Ninth International Conference on Information Technology - New Generations, Las Vegas, NV, USA, 2012, pp. 466-471, doi: 10.1109/ITNG.2012.107..

[2] A. Lotfy, S. F. S. Farooq, Q. S. Wang, S. Yaldiz, P. Mosalikanti and N. Kurd, "A system-verilog behavioral model for PLLs for pre-silicon validation and top-down design methodology," 2015 IEEE Custom Integrated Circuits Conference (CICC), San Jose, CA, USA, 2015, pp. 1-4, doi: 10.1109/CICC.2015.7338432.

[3] Peng, S. Z., Zhang, Y., Wang, M. X., Zhang, Y. G., & Zhao, W. (1999). Magnetic tunnel junctions for spintronics: Principles and applications. Wiley Encyclopedia of Electrical and Electronics Engineering, 1-16. https://doi.org/10.1002/047134608X.W8231.

[4] Vatajelu, E. I., Rodríguez-Montañés, R., Di Carlo, S., Indaco, M., Renovell, M., Prinetto, P., & Figueras, J. (2015, May). Power-aware voltage tuning for STT-MRAM reliability. In 2015 20th IEEE European Test Symposium (ETS) (pp. 1-6). IEEE. https://doi.org/10.1109/ETS.2015.7138748.