

# mL: Shrinking the Verification volume using Machine Learning



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INTRODUCTION

Hardware design verification uses Constrained Random Testing (CRT) [1], where the test inputs are generated randomly. These tests may end up wasting compute in scouring healthy regions of design, that have already been tested in past regressions.

Using Machine Learning (ML), we classify randomly generated tests on their likelihood of failing/passing pre-simulation. Based on this classification we run more efficient regressions.

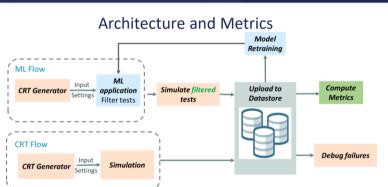
Train Data	Retrain Frequency	Input	Output
2 weeks of regression data Input	Weekly	Test knobs	Test Fail/Pass Decision

Continually changing design necessitates ML retraining periodically to keep the models relevant to the underlying RTL.

Test #	Knob-1	Knob-2	 Knob-p	Fail
Test_1	Val-1_1	Val-1_2	 Val-1_p	True
Test_2	Val-2 1	Val-2 2	 Val-2 p	False
:	1	1	 :	:
Toot n	Vol n 1	Vol n 2	Vol n n	False

 Test\_n
 Val-n 1
 Val-n 2
 ....
 Val-n p
 rate

 Table 1: Simulation test data structure for training. n=1 million, p=1000



Note: ML and CRT flows need to run together for retraining data generation and exploring unexplored design regions

**CONCLUSIONS** 

Quality

1.6x

CHALLENGES

· Class Imbalance - The number of fails and passes present in our training

• ML development during live projects get limited budget for experiments.

• ML is a science of probability and hence comes with a margin of

data are highly imbalanced (5:95). Hence, we use gradient boosted training

Efficiency Metric (UFS per CPU\_Hour) Number of Unique Fail signatures found in 1 CPU Hour spent by either flow.

6

AUTOMATION

Efficiency

1.35x

algorithms which handle class imbalances well.

· Adaptability to project phases and the verification strategy.

approximation. It's hard to reason for ML picking a test stimulus.

Quality Metric (UFS Recovery Rate) Given 1 CPU hour, what portion of design UFS's are found by ML and CRT flows. Cost Saving Metric Compute saved by ML in finding the UFS's it found, which in an ML absent scenario would have to be found by CRT.

Cost

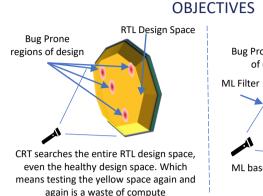
Savings

7.6%

Data Driven

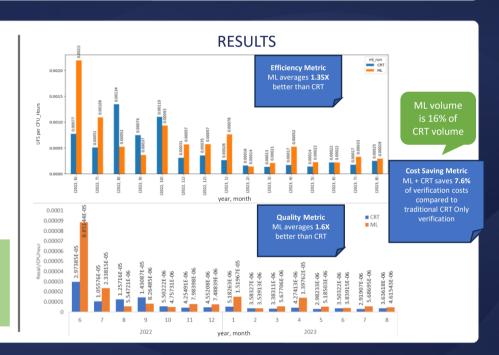
Processes and

Improvements



RTL Design Space Bug Prone regions of design ML Filter ML based filter prunes inefficient tests that waste compute (green area)

The objective is to use an ML based predictive filter, before simulating tests on the design. As illustrated in the above example, the ML filter would prevent from running tests classified to the healthy region of the design. In this way we run smaller, more efficient regressions and save compute.



## FUTURE WORK

#### **Deployment Improvements:**

- 1.Find ML:CRT tests ratio for best savings by the phase of the project? 2.Find the best ratio of generated test to the no. of filtered tests for ML? Machine Learning Improvements:
- 1. Tune ML models feature selection, other training algorithms, creation of better Cross Validation scoring functions etc.
- 2.Use ML to find efficient test set for quantifying RTL coverage.
- 3. Using generative AI to control knob generation and hit bug prone test knobs.

### REFERENCES

 [1] Constrained Random Verification, Yuan J.; Pixley, C.; Aziz, A.; 2006, XII, 254p. 72 Illus., Hardcover, ISBN: 978-0-387-25974-5

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**Preprocessing** - H. Shin, "Data-Centric Machine Learning Pipeline for Hardware Verification," 2022 IEEE 35th International System-on-Chip Conference (SOCC), Belfast, United Kingdom, 2022, pp. 1-2, doi: 10.1109/SOCC56010.2022.9908095.

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