Accelerated Verification of NAND Flash Memory using HW Emulator

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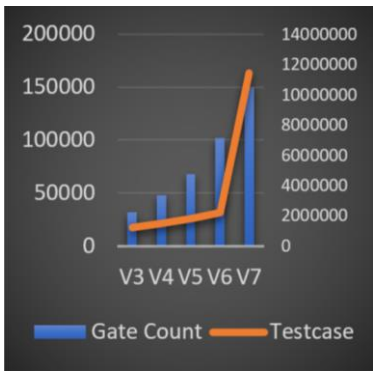
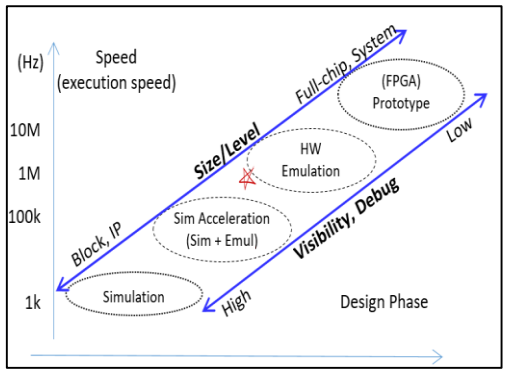
INTRODUCTION

In NAND Flash Memory, logic design becomes more complex as generations go by, and verification test cases are also increasing. In order to overcome the above situation, a verification methodology using an emulator rather than a verilog simulator is needed.



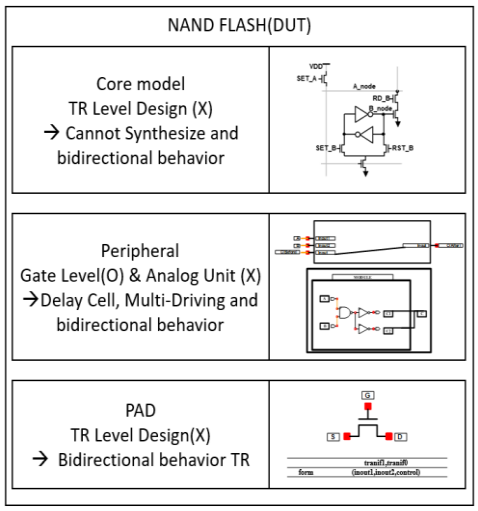


OBJECTIVES

Emulator not Supported.

- Bidirectional Transistor
- Bidirectional Behavior
- Non-Synthesizable Code
- # Delay
- Multi-driving signal
- Combinational Loop
- Strength Limited support
- Unknown(x)/high-z(z)

NAND Flash Designed by Gate & Transistor Level



METHOD

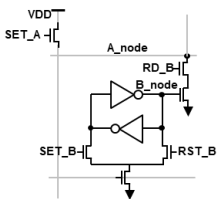
1. Synthesizable Model Development of various design style.

Change bidirectional transistors/ports to unidirectional.

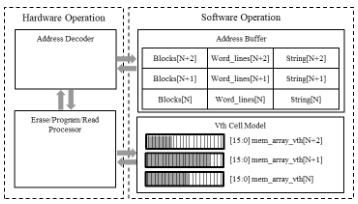
Create or change synthesizable code for Analog Unit

Remove multi-driving signal

2. Core operation Behavior Model



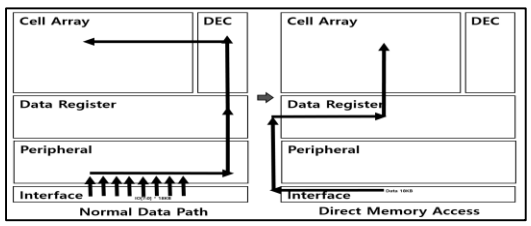

```
always @(SET_A) begin
   A_node <= 1 ;
end
always @(RD_B) begin
   A_node <= A_node & (~B_node) ;
end
always @(SET_B) begin
   B_node <= A_node | B_node ;
end
always @(RST_B) begin
   B_node <= (~A_node) | B_node ;
end
```



METHOD

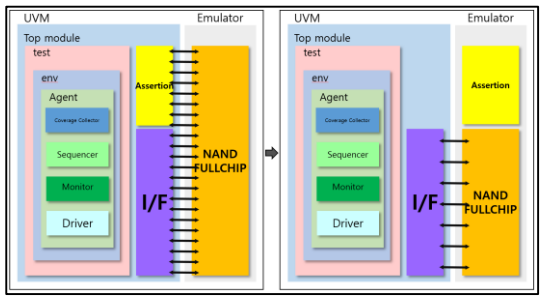
3. Emulation performance improvement skills.

- Direct Memory access



- Interface optimization

- Assertion Checker move



RESULTS & CONCLUSIONS

Can verify more complex Flash memory behavior.

Simulation Condition	Verilog Simulation	Emulation	Rate
Data Size 18KB	3751h	7857.8h	X0.47
Data Size 18KB, Memory Direct Access		186h	X20.2
Data Size 18KB, Memory Direct Access, Interface optimization		42h	X89.3
Data Size 18KB, Memory Direct Access, Interface optimization, Assertion Checker move		37h	X101.4

	Verilog Simulation	Emulator Simulation
Compile Time	0.3h	2.5h
Run time	3751h	37h
Dump Time	5179h	283h

Performance Comparison (Total case: 5000)

REFERENCES

[1] Transaction-Based Simulation Acceleration for SSD Controller Using HW Emulator, Samsung, 2021.

[2] Cadence Emulator Manual. (vxeUser Guide).

[3] Cadence UVMA Manual.

[4] Nayoung Choi, et al., "Modeling and simulation of NAND flash memory sensing systems with cell-to-cell V_{th} variations," ICCAD: Proceedings of the 39th International Conference on Computer-Aided Design November 2020 Article No. 52 Pages 1–8, Dec. 2020.

[5] K. Parat and A. Goda, "Scaling trends in NAND flash," in Proc. of IEEE Int'l Electron Devices Meeting (IEDM), pp. 2.1.1-2.1.4, Dec. 2018.

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