On Analysis of RDC issues for identifying reset tree design bugs and further strategies for noise

Farhad Ahmed, Lyle Benson, Manish Bhati

Siemens Industry Software Inc.

accellera SYSTEMS INITIATIVE

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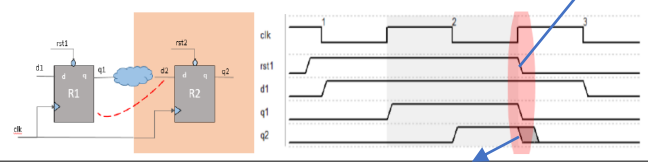
INTRODUCTION

RDC Paths Cause Metastability

- Between two registers having a data path whose resets are different and asynchronous but have same clock domain
- Reset assertion value from source register propagates to destination register may cause metastability

‘rst1’ asserted very close to ‘clk’ posedge



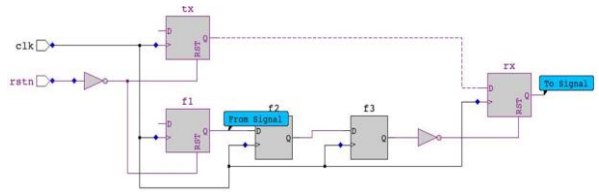
‘R2’ flop output goes metastable due to setup/hold time violation

MOTIVATION

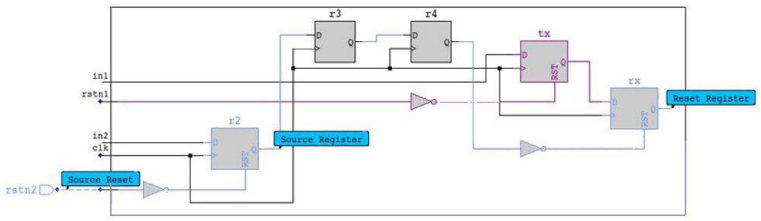
- Independent reset domains can give rise to metastability
- The metastability induced by asynchronous reset structures can not be modeled accurately in simulation
- Increasing reset domain complexity demands exhaustive RDC analysis at early stage of RTL designs
- EDA vendors continue to add newer checks and methodologies in the static analysis tools (CDC, RDC) to help engineers investigating complex reset schemes in the design
- Left unchecked, there is considerable risk of unpredictable chip behavior when samples come back

NRR ON ASYNCHRONOUS RESET PATH

Case Study #1: Both Source and Destination registers have *same* asynchronous reset source. If time delays through the NRRs are not accounted for, RDC analysis tools could incorrectly identified the path between registers as a synchronous reset path

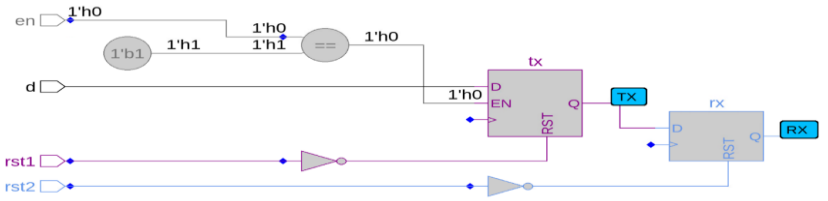


Case Study #2: Both Source and Destination registers have *different* asynchronous reset sources. Even with correct reset order constraint, due to the presence of NRRs, an RDC path may exist between the source register “tx” and the destination register “rx”

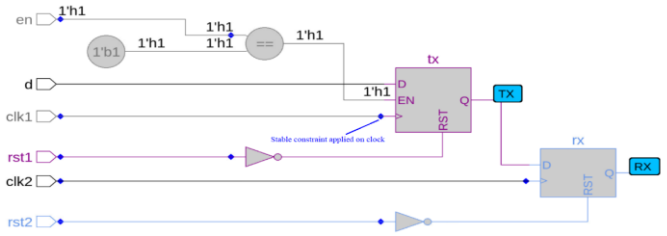


NOISE MANAGEMENT IN RDC ANALYSIS

Case Study #1: The “en” pin of the source register is tied to constant zero, making this register stable. RDC Analysis infers these types of paths as stable and puts them in a separate RDC scheme

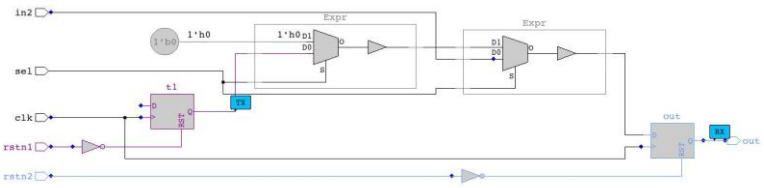


Case Study #2: The clock pin of the source register, “clk1”, is constrained as a stable signal. RDC tool infers these types of paths as stable and puts them in a separate RDC scheme

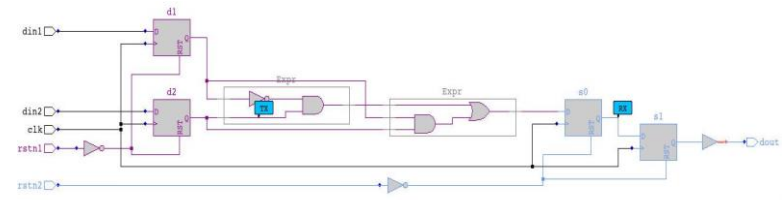


AUTOMATIC RECOGNITION OF FFP IN RDC ANALYSIS

Case Study #1: RDC crossing exists between the source register “t1” and destination register “out”. But due to two MUX logics on the data path, the path between the registers are considered functionally false



Case Study #2: Boolean optimization of the combinational logics is simplified to [(!din1 & din2) + (din1 & din2)) => ((!din1 + din1) & din2)] => din2. So, path between “din1” and “out” is a FFP.



CONCLUSION

- Scalability: This analysis was done on one of the largest DUTs in the world for a large WW processor company.
- We have highlighted specific issues to improve RDC results and to ensure the highest fidelity in identifying real design issues
- Presence of NRRs in the reset tree may pose a risk due to timing delays in the reset tree that can manifest themselves by creating an asynchronous reset behavior even with same reset sources for the TX and RX registers
- Tool-provided constraints should be preferred for doing noise management in RDC analysis
- We have demonstrated how to reduce noise in CDC/RDC analysis by identifying the paths that can be filtered from the results analysis through the inference of stable properties, due to contributing constants, and combinatorial paths using automated formal analysis techniques
- Engineers writing RTL often don’t realize that some RDC paths are functionally false paths. We have shown how functional false paths can be identified using automated formal techniques so engineers can focus on real design bugs

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Authors’ contact information

farhad.ahmed@siemens.com

lyle.benson@siemens.com

manish.bhati@siemens.com