Reset Sweep Verification for Elimination of Reset Domain Crossing Blind Spots in Design

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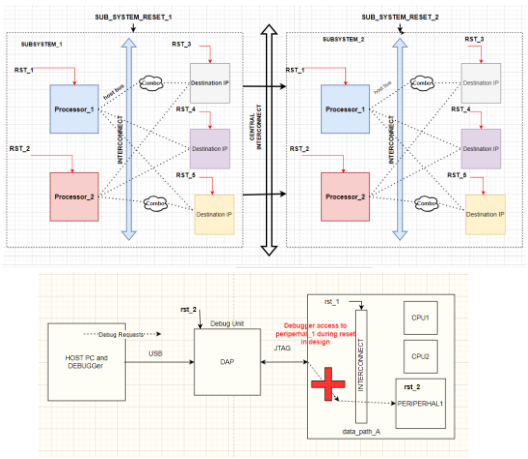
PROBLEM STATEMENT

- Conventional RDC checks are not 'ENOUGH'
- Analyzing & disposing of 1000000s of RDC violations heavily manual & error prone
- Potential risk of losing 'in-flight' data or system hangs due to RDC on partial reset assertion
- SDV architecture => multiple new Software Reset Domains => increase in RDC complexity

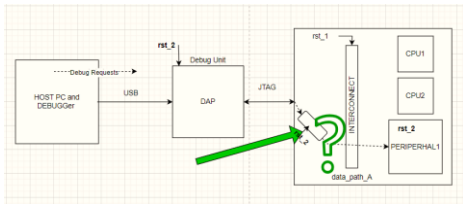


Blind Spot RDC Silicon Bug!

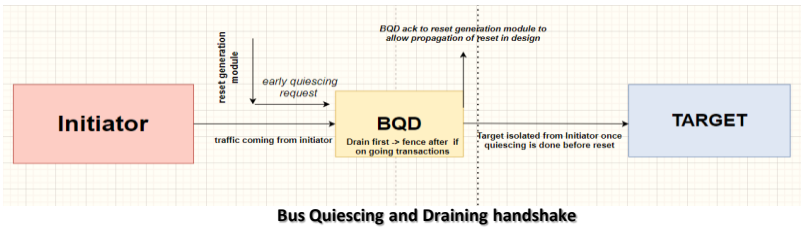
NOVEL ARCHITECTURE AND DESIGN

Architecture & Design

- Bus Quiescing and Draining logic (BQD) gaskets across the RDC's path where the source, destination and operating path are operating on different reset domains

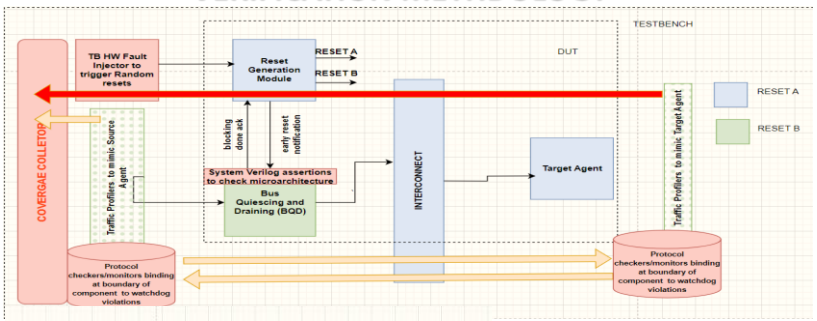


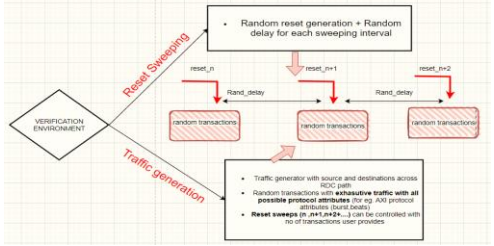
Quiescing & Draining logic needed here!



Bus Quiescing and Draining handshake

VERIFICATION METHODOLOGY



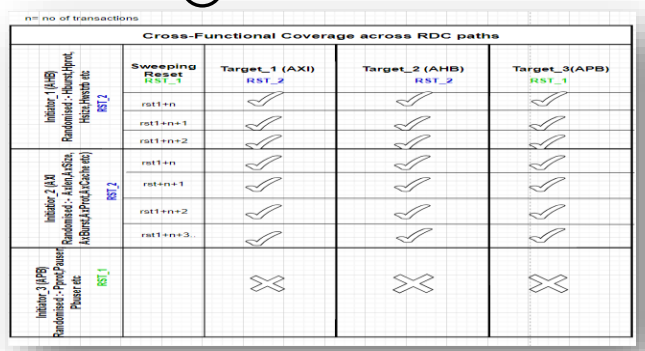


Reset Sweep Verification

Focused RDC Verification

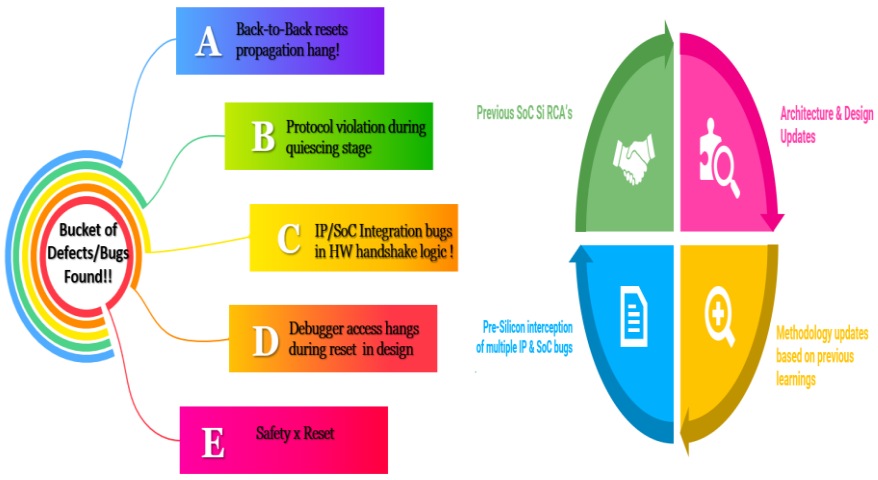
- Bus Functional Model (BFM) traffic profile driver generates random heavy bus traffic
- Randomized initiator attributes
- Reset Sweeping across bus traffic with random delays

RESULTS



Simulation Result

CONCLUSIONS



Classification of bugs intercepted

FUTURE WORK

- Stitching Machine learning or data modelling in same setup can be investigated to make it automated and more efficient as scope of improvement.
- Quiescent Formal Checks explained in [5] can be integrated with current setup to increase robustness and catch bugs early.

REFERENCES

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[6] I. Ahmed, K. Nouh, and A. Abbas, "Multiple Reset Domains Verification Using Assertion Based Verification," in Proceedings of the IFIP/IEEE International Conference on Very Large-Scale Integration (VLSI-SoC), 2017.
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