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Refinable Macros and Terminal Boundaries in UPF 4.0: Empowering Soft IPs of the Future

Non-Intrusive Refinements for Seamless Soft IP (SIP) Integration

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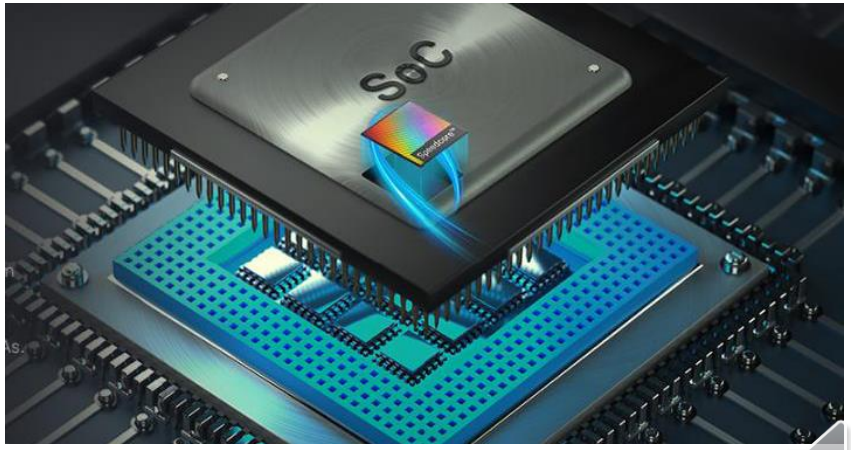
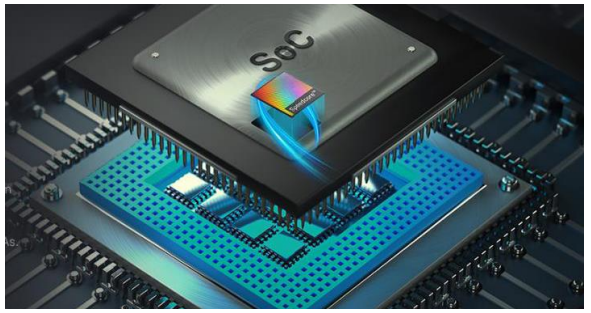
accellera SYSTEMS INITIATIVE

Agenda: Solving the SIP Integration Puzzle

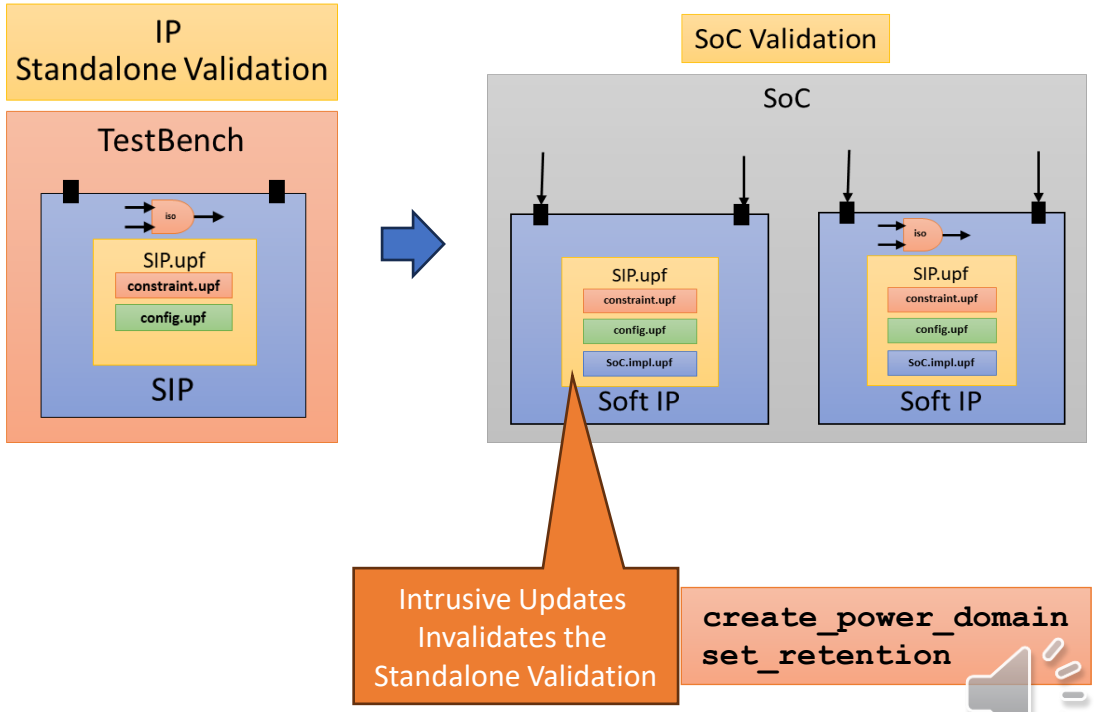
- **The Problem**
  - SIPs vs. SoC Constraints
- **UPF 3.1**
  - Progress & Gaps
- **UPF 4.0**
  - Refinable Macros to the Rescue
- **Case Study**
  - Optimizing Without Breaking Trust
- **Future-Proofing SoC Design**



The SIP Integration Challenge

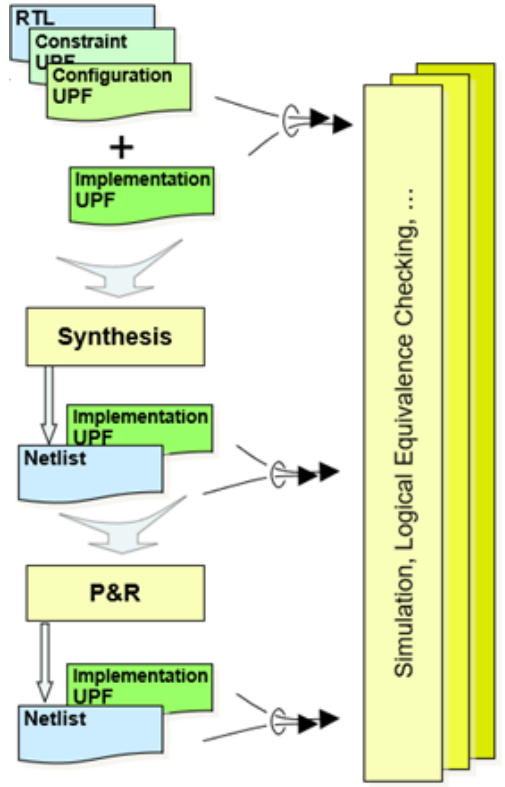


- **SoC Complexity**
  - 50+ SIPs, each with unique power rules
- **The Dilemma**
  - **Modify** SIPs -> risk introducing bugs
  - **Revalidate** SIPs -> wastes time
- **UPF 3.1's Fix**
  - Good for implementation
  - Too rigid for verification



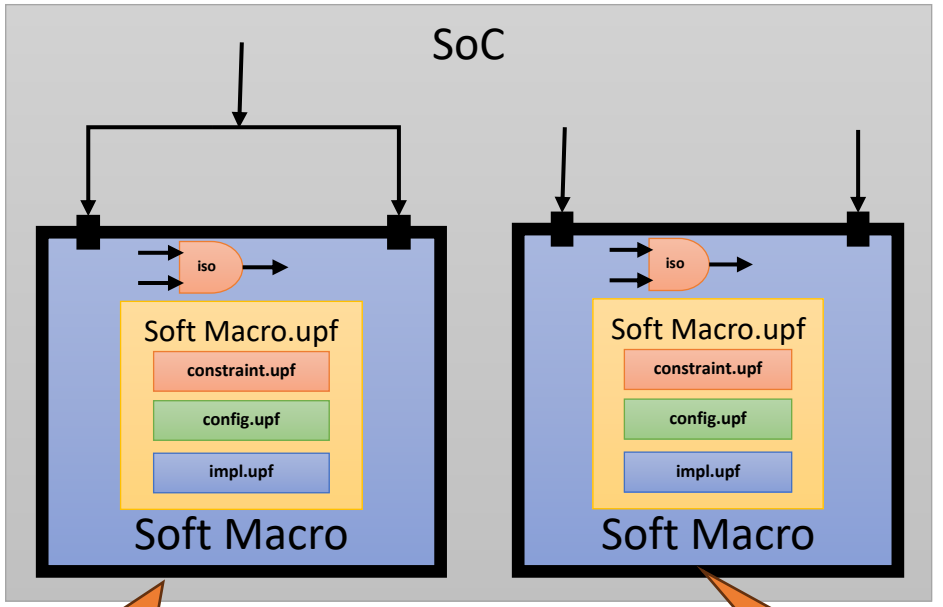
UPF 3.1 : Progress and Gaps

- **Successive Refinement**
  - Layered power intent
  - Constraint -> Configuration -> Implementation



UPF 3.1 : Progress and Gaps

- **Successive Refinement**
  - Layered power intent
  - Constraint -> Configuration -> Implementation
- **Soft Macros**
  - IPs as locked boxes (Terminal Boundaries)
  - Bottom-Up Implementation Focus
- **The Gap**
  - No safe way to adjust boxes post - integration

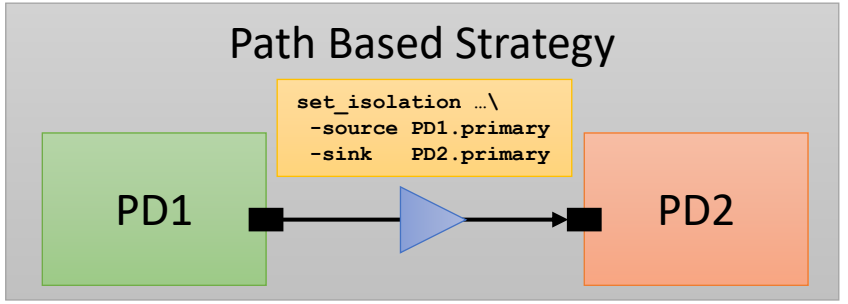


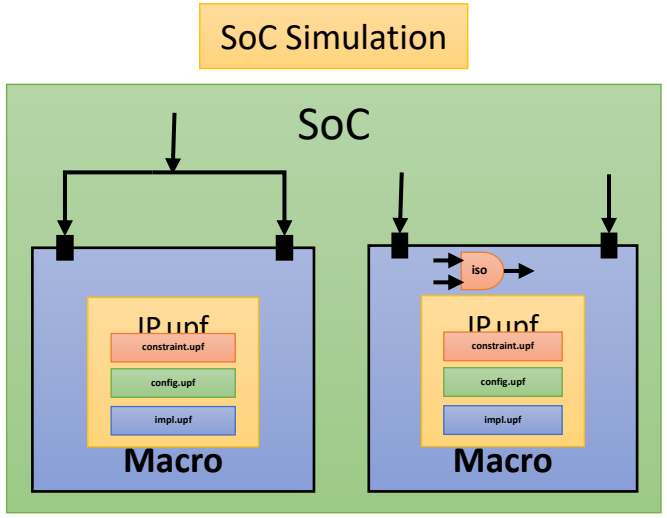
STRICT
TERMINAL BOUNDARIES

Pre-Hardened outside SoC
No logic optimizations

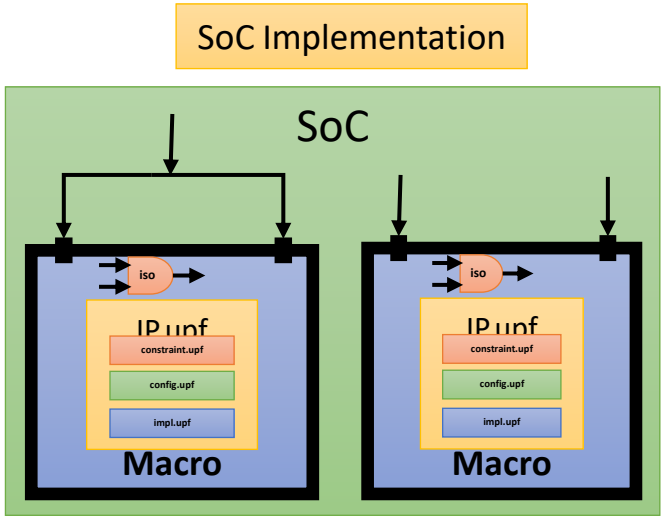
Path Based Strategy Mismatch: Simulation vs. Synthesis

- **Path Based Strategies**:
  - Insert cells based on connectivity
  - Automate power-management cell insertion
  - Pose problems for IPs
- **Scenario**:
  - IP with 2 Supplies
  - SoC Shorts One Instance
- **Problem**: Simulation Omits Isolation, but Synthesis Retains Isolation
- **Terminal Boundaries** mitigate these mismatches in UPF 3.1





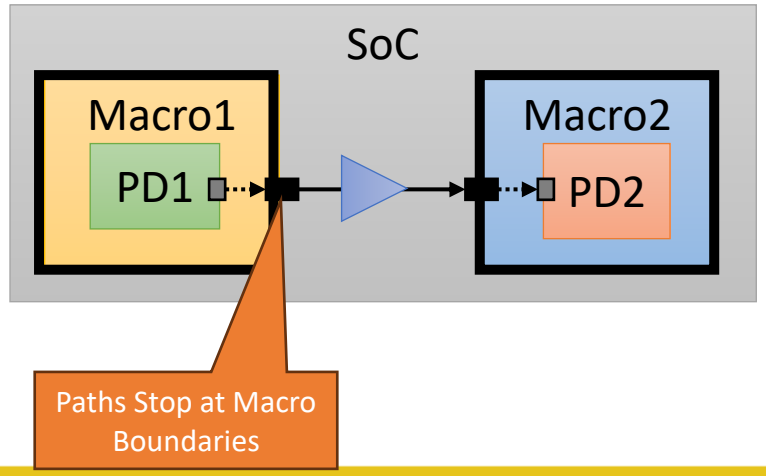
Simulation will not see Isolation Cell
In the instance where supply is shorted



Macro synthesized as standalone block
SoC reuses netlist of Macro regardless
Both Instance of Macro have isolation cells

Terminal Boundaries: Guarding the IP Fortress

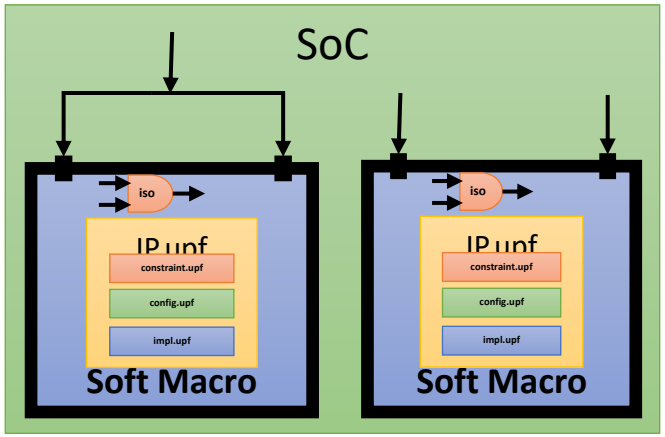
- **Protects** IP from External Overrides
- Path-Based strategies **respect** the boundary
- **Boundary constraints** are user defined and **Tool-Validated**
- **Essential** for Consistent Interpretation, but can be limiting



Soft Macros : Bottom-Up Implementation

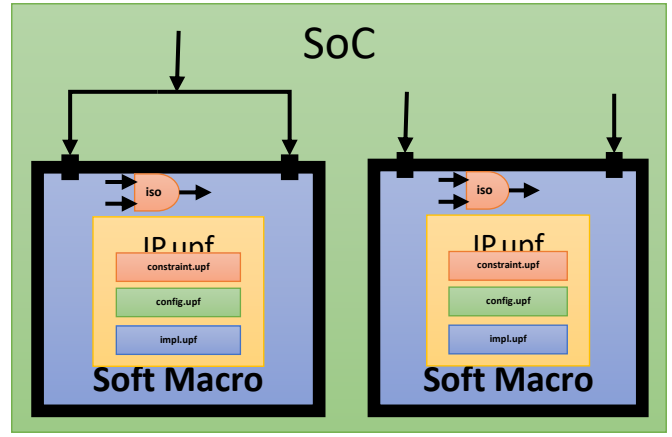
- Create Terminal Boundaries for implemented blocks
- **Pros**
  - Preserve IP integrity
  - Ensure consistent Simulation vs Synthesis semantics
- **Cons**
  - Rigid Terminal boundaries
  - No refinements
- Not suited for preverified SIPs
  - Intrusive updates break standalone validation

SoC Simulation



Simulation mimics the Synthesis Behavior
Because of Soft Macro marking

SoC Implementation



Macro synthesized as standalone block
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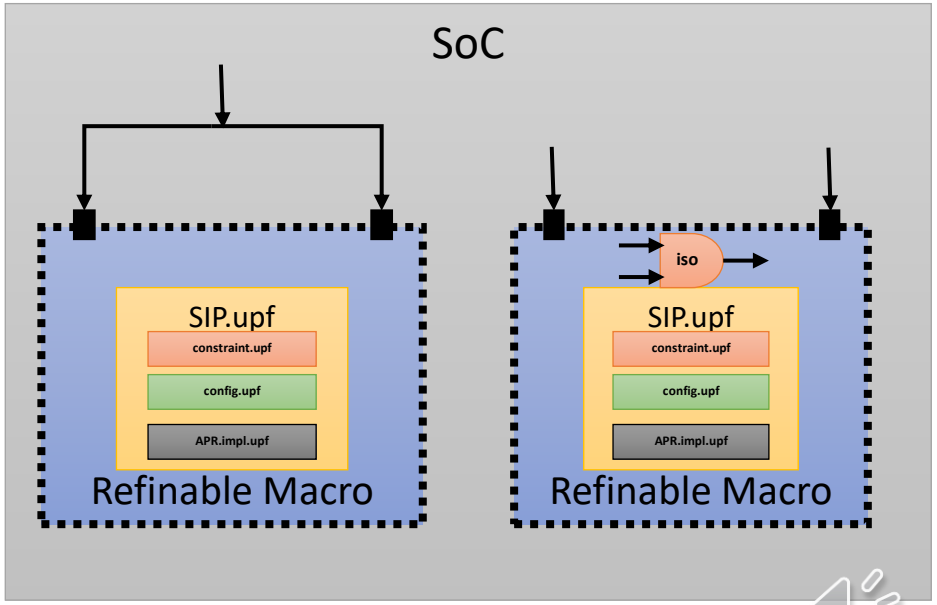
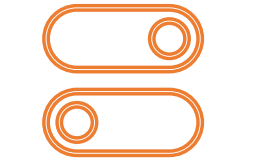
Refinable Macros in UPF 4.0

- Refinable Terminal Boundaries
- **Tool-Enforced Safety**
  - Non-Intrusive Power Intent Updates
- **Preserved Verification**
  - Original IP UPF remains untouched
- **Enables** System-Level **Optimization** during Implementation
- Ideal for Bottom-Up Verification



Coding Refinable Macros

- Simple UPF Attribute
- Mark IP internally or externally
- Maintains IP Verification
- Override to Soft Macro if Needed



Mark IP as Refinable Macro

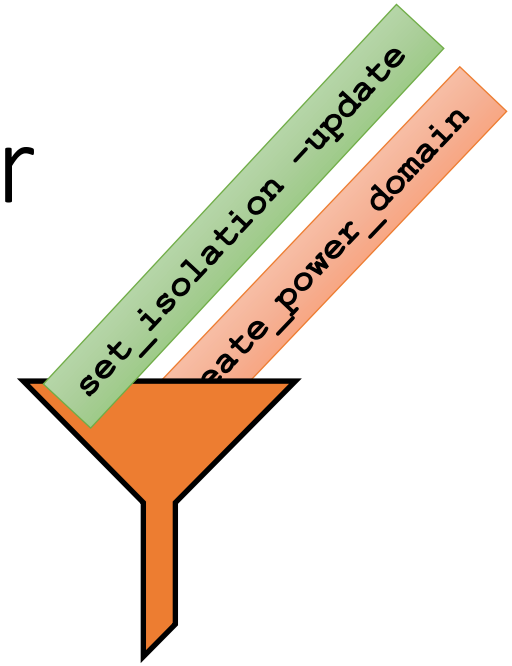
Safe Updates

Preserves Verification

```
# Mark directly in IP UPF:
set_design_attributes -models . -is_refinable_macro true

# Or mark externally:
set_design_attributes -models IP_Design -attribute {UPF_is_refinable_macro TRUE}
```

Implementation UPF : The Safety Filter



- **Safe Refinements** via Allowed Commands and options
  - UPF 4.0 defines allowed commands and options
- -implementation Enforces **Correct-by-Construct** UPF
  - EDA Tools Enforce Compliance
- **No Alteration** of Original IP UPF
- **Preserves Verification** Integrity

```
# SoC UPF
load_upf ip_impl.upf \
   -scope myIP \
   -implementation

# ip_impl.upf
set_isolation PGD_to_AON \
 -domain PGD \
 -location parent
 -update
```

Practical Example: Refinable Macros in Action

ip.upf

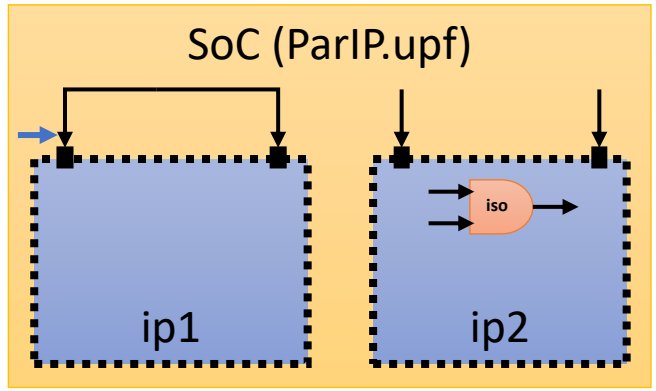
```
set_design_attributes -models . \
-is_refinable_macro TRUE

create_supply_set ss_IP_AON
create_supply_set ss_IP_PGD

create_power_domain AON -elements {.}
create_power_domain PGD -elements
{ip1_pgd_wrapper}

## Isolates all outputs where different
## supplies power source and sink
set_isolation PGD_to_AON -domain PGD \
 -isolation_supply_set ss_IP_AON \
 -applies_to outputs -source ss_IP_PGD \
 -diff_supply_only TRUE \
 -isolation_signal pwr_manager/iso_en_b \
 -isolation_sense low
```

AON and PGD supplies are shorted for one instance of the IP



ParIP.upf

```
create_power_domain par_AON -elements {.}
create_supply_set ss_SOC_AON
create_supply_set ss_SOC_PGD

load_upf ip.upf -scope ip1
load_upf ip_impl.upf -scope ip1 -implementation
associate_supply_set {ss_SOC_AON ip1/ss_IP_AON}
associate_supply_set {ss_SOC_AON ip1/ss_IP_PGD}

load_upf ip.upf -scope ip2
load_upf ip_impl.upf -scope ip2 -implementation
associate_supply_set {ss_SOC_AON ip2/ss_IP_AON}
associate_supply_set {ss_SOC_PGD ip2/ss_IP_PGD}
```

ip_impl.upf

```
set_isolation PGD_to_AON \
 -domain PGD \
 -location parent
 -update
```

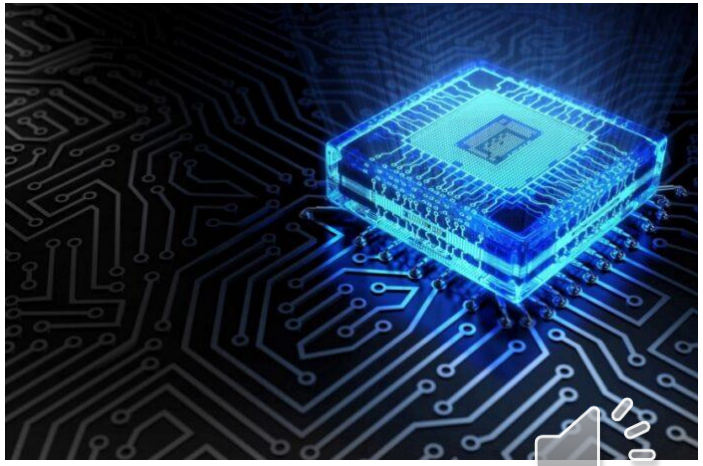
Implementation updates only

Guidelines & Best Practices

- **Always mark terminal boundaries**
- **Use Refinable Macro Marking for SIPs**
- **Keep Original IP UPF Intact; add SoC adjustments in Implementation UPF**
- **Leverage –implementation for Correct-by-Construct**

Conclusion: Empowering Soft IPs of the Future

- **Terminal Boundaries -> Unified Tool Behavior**
- **UPF 4.0 -> Bridges SIP Verification Gaps**
- **Refinable Macros = Flexibility + Safety + Performance**
- **Implementation UPF -> Correct-by-Construct**
- **Preserves Verification & Saves Time**



Acknowledgements

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Thank you

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