Shift-Left on Timing Constraints Verification: Beyond Typical Front-End Execution

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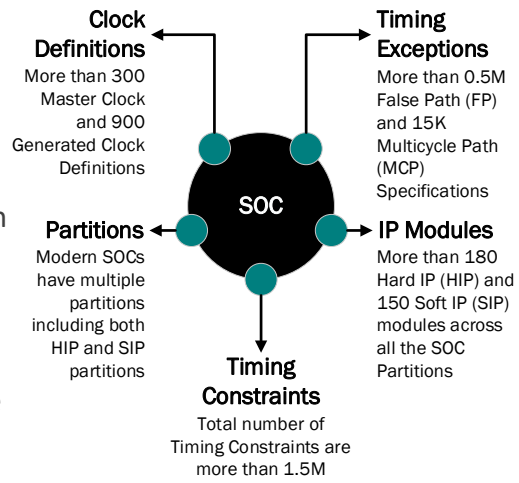
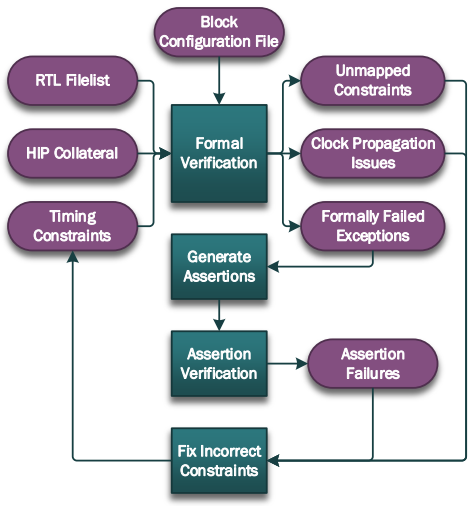
INTRODUCTION & BACKGROUND

- Accuracy of timing constraints is critical for proper synthesis results and timing closure of modern-day SOC designs
- Gate-Level Simulation (GLS) is traditionally used to verify the timing constraints, but it occurs too late in design cycle, has long turnaround time and offers less coverage



TIMING CONSTRAINT VERIFICATION METHODOLOGY

- Primary Inputs are RTL File List, HIP Collateral, Timing Constraints and Block Configuration File
- Ensure 100% Timing Constraint Mapping
- Ensure Zero Clock Propagation Issues
- Formal Verification and Assertion Generation
- Assertion Verification in Functional Simulation



FORMAL VERIFICATION RESULTS

- 100% Constraint Mapping & Zero Clock Warnings at RTL1P0
- 74.36% Generated Assertion reduction by implementing formal verification improvement techniques
- Formal Verification Improvement Results

#	Formal Verification Improvement Techniques	No. of Assertions	Assertion Reduction %
1	Flat Run	508999	0.00%
2	Adding Synchronizer Cell Specification	506554	0.48%
3	Adding Input Port Constraints	455080	10.59%
4	Adding Asynchronous Reset Constraints	269077	47.13%
5	Importing CDC Constraints	135435	73.39%
6	Adding Static Signal Constraints based on Uncovered Assertions	130491	74.36%

TIMING EXCEPTION VERIFICATION RESULTS

- SOC MCP Exception Formal Verification Results

% of PASSING MCPs	% of FAILING MCPs	% of NO PATH MCPs	% of SKIPPED MCPs	% of WAIVED MCPs
66.17%	12.40%	18.18%	2.85%	0.40%

- SOC Functional (non-DFX) MCP Exception Assertion Simulation Verification Results

No. of Assertions Generated corresponding to Functional (non-DFX) MCPs	No. of PASSED Assertions	No. of FAILED Assertions	No. of UNCOVERED Assertions	No. of MCPs corresponding to Assertion Failures
4588	1385	154	3049	7

CONCLUSIONS & FUTURE WORK

- Proposed methodology is faster, scalable and more efficient than conventional methods (such as GLS)
- Achieved significant noise reduction in timing exception verification by identifying and excluding all the timing exceptions that do not require verification upfront (such as NO PATH, SKIPPED, WAIVED exceptions)
- Identified and fixed all the incorrect MCP exceptions before timing closure of the design, thereby preventing any potential silicon bug escape and costly re-spin of the silicon
- Future efforts will focus on expanding the assertion verification to include DFX-related MCPs. The future plans also include extending the entire methodology for False Path (FP) verification as well.

REFERENCES

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[2] A. Khandelwal, A. Gaur and D. Mahajan, "Gate level simulations: verification flow and challenges," EDN, 5 March 2014. [Online]. Available: https://www.edn.com/gate-level-simulations-verification-flow-andchallenges

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