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Reuse of System-level Circuit Models in Mixed-Signal Verification

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Agenda

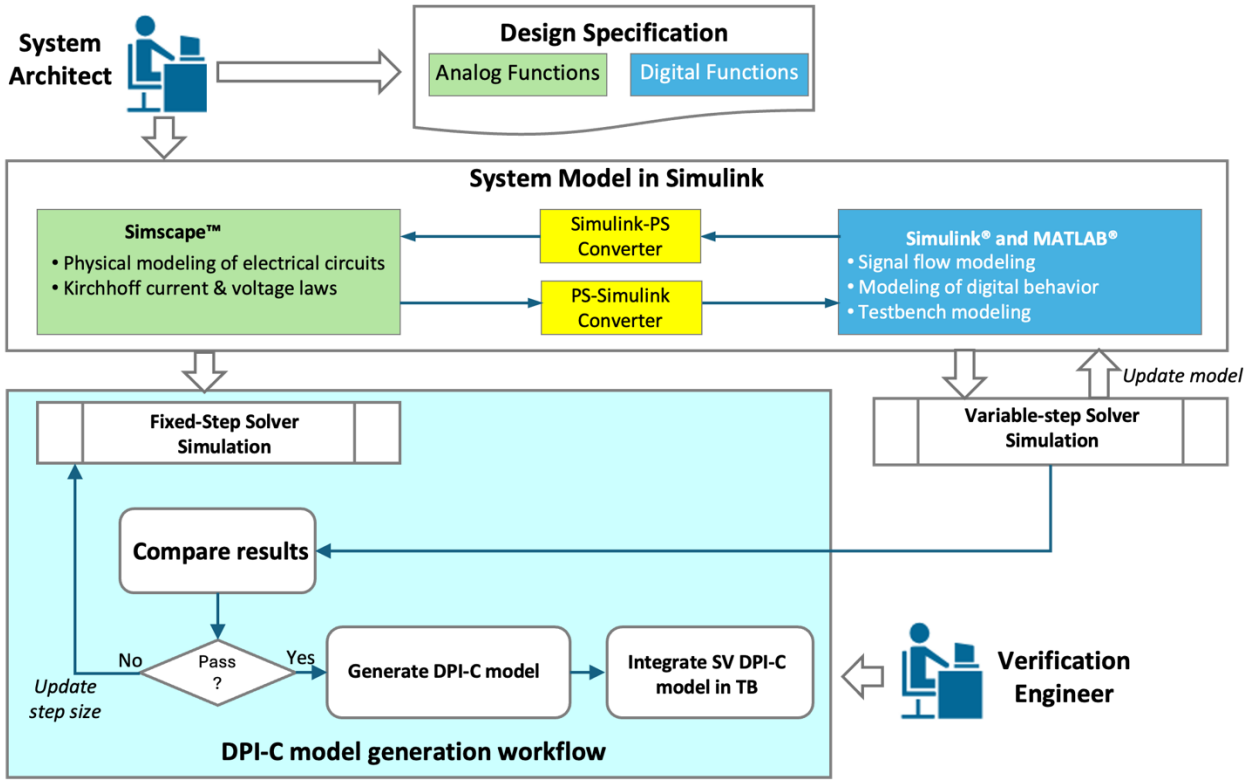
- Motivation
- Proposed workflow
- Use cases
- Results
- Limitations
- Conclusion

Motivation

- Analog models developed after design definition
- SV-RNM/SV-UDT or Verilog-AMS models require design knowledge and significant effort to develop and verify to achieve accuracy while maintaining fast simulation speeds
- System models are built for architecture exploration, definition and refinement
- Reuse of existing models can bridge the model availability gap

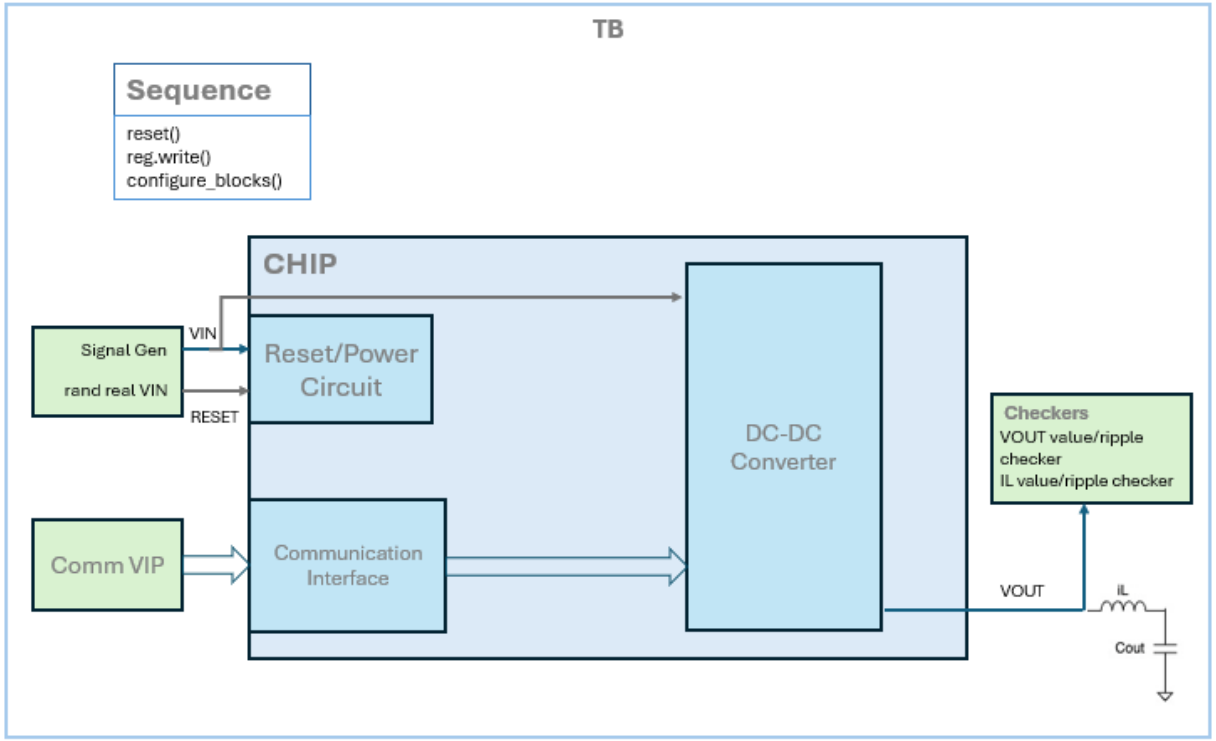
Proposed Workflow

- To develop system models, Architect uses
  - Simulink® for signal flow modeling
  - Simscape™ for electrical modeling
- Models simulated to prove architecture feasibility
- Design proceeds with implementing the proposed architecture
- Verification leverages proven models for various use cases



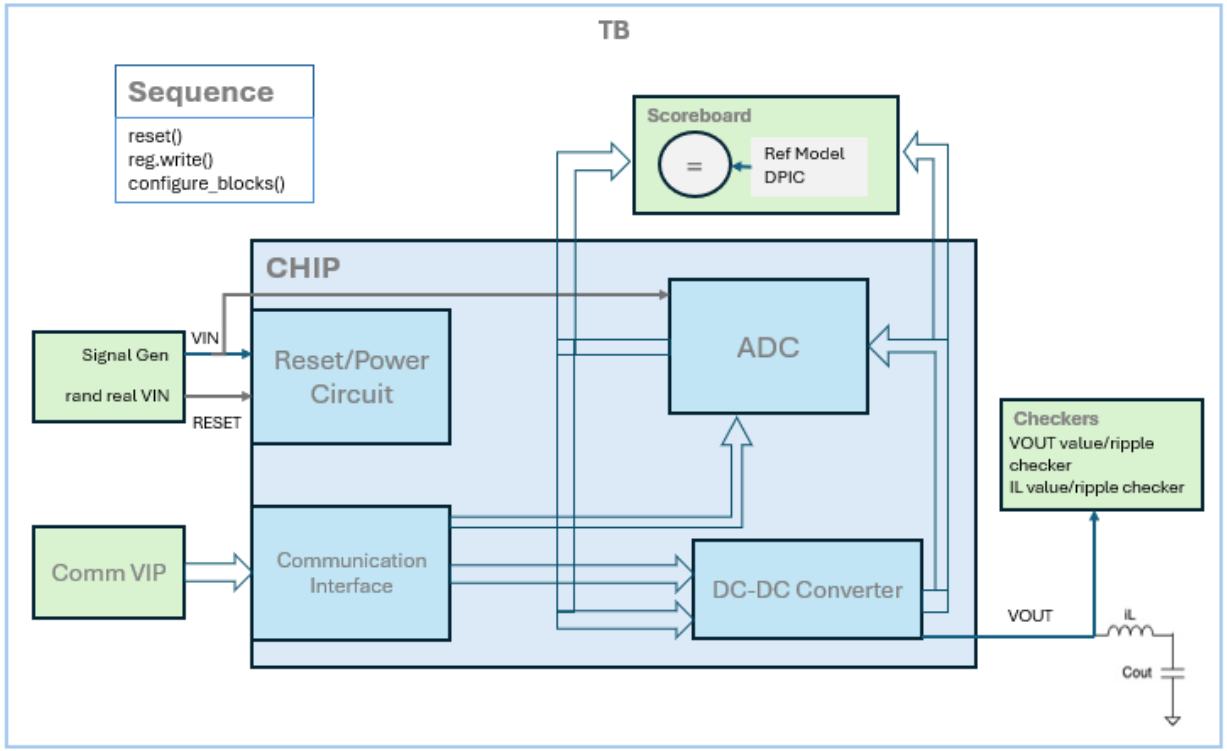
Use case 1 – Environment Bring-up

- DPI-C generated models used for TB and tests development
- Model represent a SystemVerilog view of empty design stubs
- Represents a full-feature behavior of the circuit behavior of DC-DC converter
- Can represent parts of the design, e.g. Buck converter



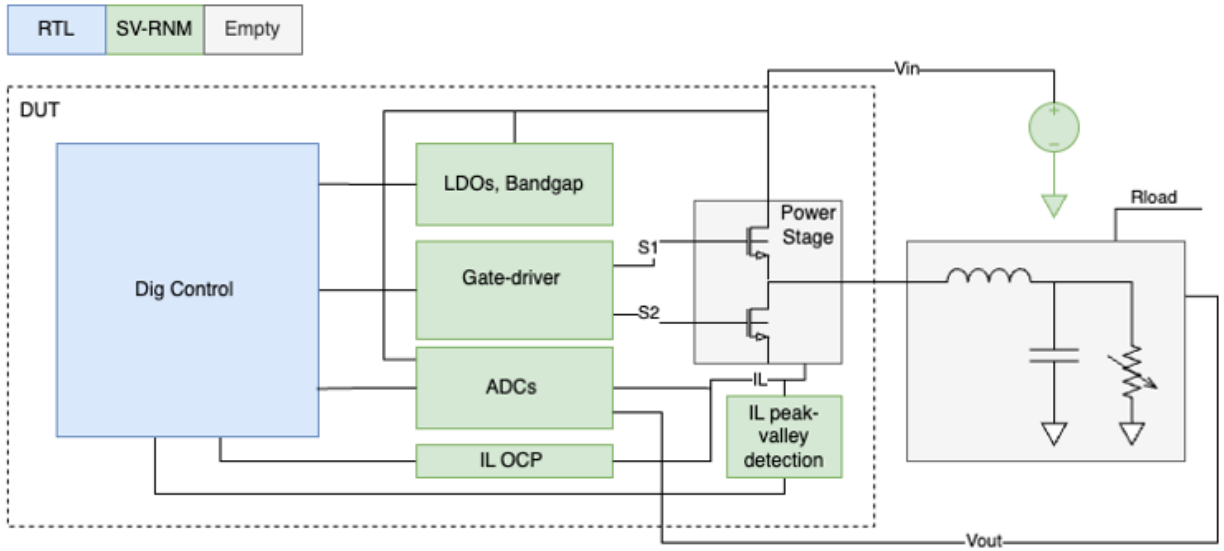
Use Case 2 – Reference Model

- DPI-C generated model used in scoreboard to generate a bit- and cycle-accurate expected value for comparison to design's output
- Agreed upon tolerance can be set to allow for analog circuit behavior



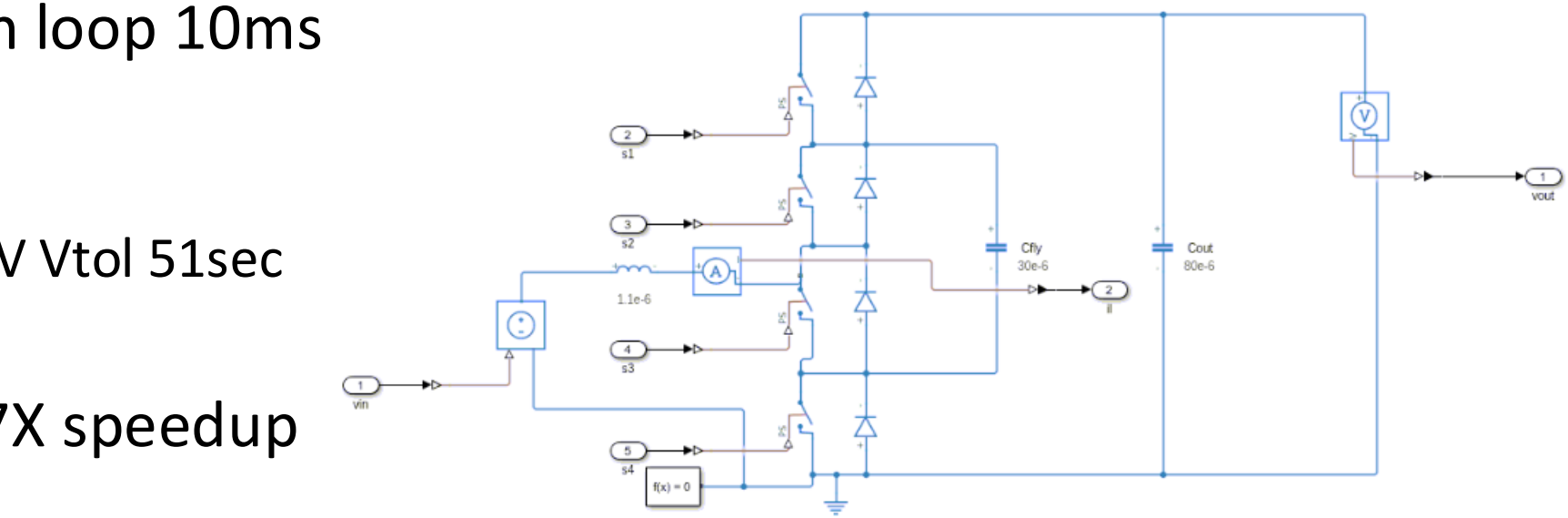
Use Case 3 – Core Model

- DPI-C generated model used as SystemVerilog view of power stage
- No custom models needed for electrical components. Use Simscape™ components



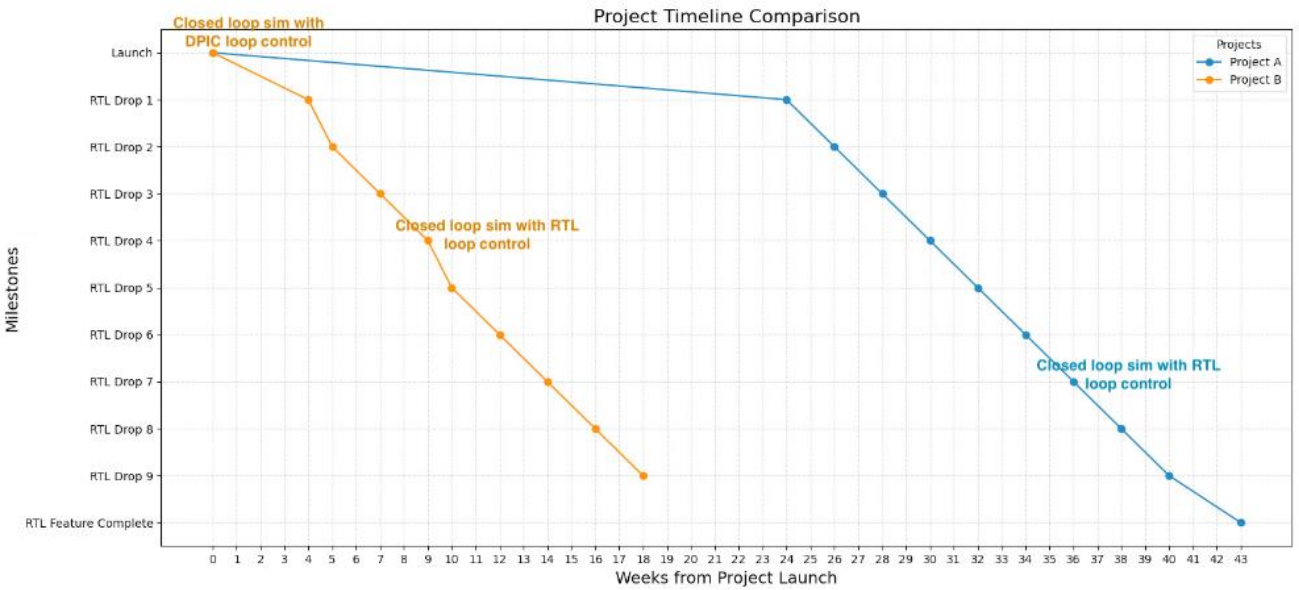
Results – Simulation Speed

- Boost 3-level open loop 10ms simulation
  - DPI-C 30sec
  - SV-UDT with 10nV Vtol 51sec
  - VAMS 54sec
- DPI-C achieves 1.7X speedup



Results - Schedule

- Project A - DV team needed to wait for the design
  - Faced delays in achieving a closed-loop simulation due to the lack of a reference
  - 43 weeks after first design drop
- Project B - DV team worked with DPI-C models generated from Simulink and Simscape
  - 18 weeks after first design drop



Limitations

- The current version of SV DPI-C models generated from Simulink® lacks support for EEnet.
- Support event-driven simulation to speed up DPI-C performance during POR, low power standby state, etc.
- Create grouped Simscape components to reduce the number of nodes (e.g., group a switch with a body diode).

Conclusion

- Reduced maintenance effort
- Consistent performance
- Faster simulation speeds
- Efficient resource utilization
- Robust debugging tools
- Collaboration between architecture and DV teams

Questions

- Thank you for attending!
- Happy to answer any questions…