A Study on Virtual Prototyping based Design Verification Methodology

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MOTIVATION

Design verification period getting shorter and shorter

- Continuous increase in HW and **SW (App.) complexity**
- Customer's demand **to shorten delivery schedule**
- The period of all design stages is getting shorter than before

Efforts to shorten the period in verification

- **Re-use** of verification environments
- **Earlier start** of verification works
- Enhancement of verification **tool performance**
- **Reduction of experiment numbers** by using A.I. and M.L.
- **M.L./A.I. based** debugging

RELATED WORKS

Virtual Prototyping (VP) & Co-Simulation

- **SystemC/TLM based Rapid Prototyping**
- **Shorter** Dev. time **/ Faster** run-time
- SystemC only and Co-sim is **faster than RTL** only sim
- C based test bench & **High reusability**

Portable Test and Stimulus Standard (PSS)

- **Re-use of verification bench** is required
- **Describe test bench and behavior once and then target it for multiple abstraction layers**
- Can **reduce verification period** dramatically by avoiding verification planning at each stage

PROPOSED METHODOLOGY

Proposed Design/Verification Flow

0. (PSS) : Test bench Reuse at Every Stage
1. (Reference) : **SystemC only** Simulation
2. (Debug) : SystemC-RTL **Co-simulation** by replacing SystemC to Verilog
3. (Confirmation) : **RTL only** Simulation

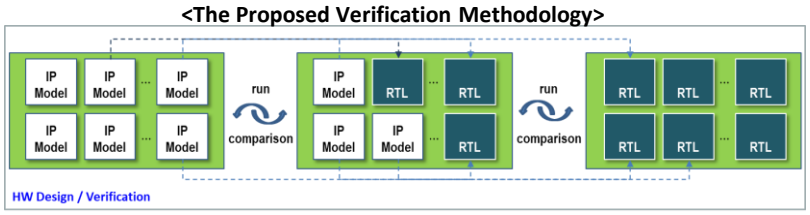
SystemC-RTL Transactors

- btw **signal level I/F** of Verilog models and **TLM I/F** of SystemC models
- Translation **by using FSM** (transaction event – signal)

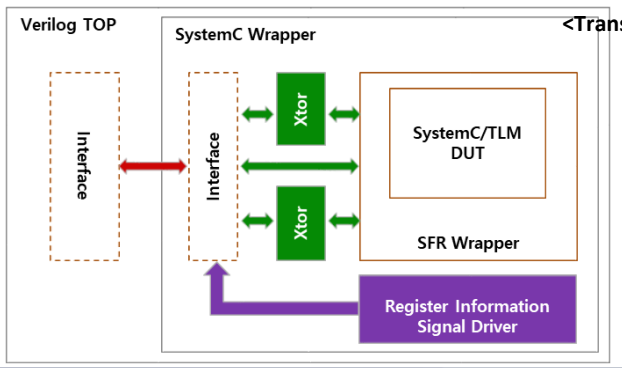
SystemC Model Structure

- **Same** operation, functionalities, hierarchy, and interfaces with RTL
- **Register Information Signal Driver** for SFR comm. with RTL
- Transactor for Protocol Translation between SystemC and RTL

<The Proposed Verification Methodology>



<Transactor Architecture>



RESULT

Test Result

- Applied to **100M G/C** mobile flagship AP SOC
- SystemC only simulation: x 5.22 faster
- Co-simulation: x1.16 faster
- **Verification period was reduced by 21% on average**

	# of IP model	Simulation Speed [MHz]		
		SystemC	Co-sim	RTL
Bus	12	4.82	0.84	0.72
		x 6.69	x 1.16	-
Memory Controller	7	4.99	1.53	1.33
		x 3.75	x 1.15	-
Avg. Improvement Rate		x 5.22	x 1.16	-

CONCLUSION

- A design verification methodology **using VP** is proposed
- Regression test was started quickly for more than a month
- **Verification period is reduced by 21% on average**

- SystemC Modeling tasks can be an overhead, the flow is performed **with other methodologies**, the developed models shares many advantages and the **overhead can be hidden**. (**Virtual Prototyping, Architecture Exploration w/ PPA**, etc.)

- **Performance/Power verification** can be performed in parallel.

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