# An Effective Digital Logic Verification Methodology of High Speed Interface IP Using a Configurable AFE Behavioral and Channel Model

Kiyoon Shim, Seungsik Eom, Beomseok Kang, Jaechul Park, Kyubeum Lee, Youngjin Chung, Hyogyuem Rhew

Samsung Electronics

accellera SYSTEMS INITIATIVE

2025 DESIGN AND VERIFICATION™ DVCON CONFERENCE AND EXHIBITION UNITED STATES

SAN JOSE, CA, USA FEBRUARY 24-27, 2025

## MOTIVATION & PROBLEM STATEMENT

### Digital Logic in Mixed Signal Design is Getting More Significant

- Logic that **estimates and compensates for Inter-Symbol Interference (ISI)** caused by an increased data transmission rate and channel loss
- Logic that **calibrates the offset** caused by mismatch of Analog Front End (AFE) device characteristics due to increased PVT variation

### Challenges in Digital Logic Verification of Mixed Signal Design

- Need repeated extraction of behavioral models for each analog characteristic
- AFE offset and ISI through the channel cannot be determined immediately
- Long simulation time due to extensive computation required to reflect the analog nature

## OBJECTIVES

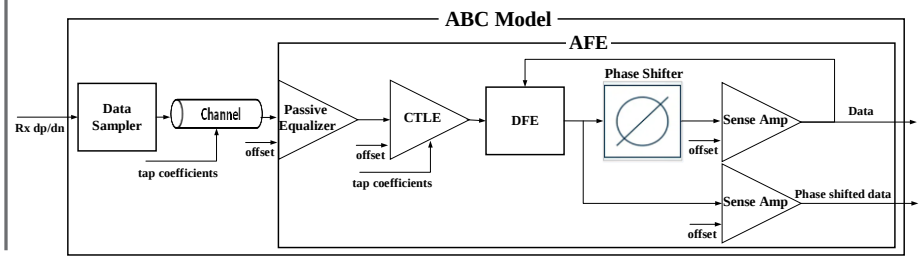
### Verification of Digital Logic

- In **various AFE and channel environments** with fast configuration
- With knowledge of the AFE offset and ISI magnitude
- With fast simulation and achieve **early bug detection**

## PROPOSED MODEL

### AFE Behavioral and Channel Model (ABC Model)

- Configurable Analog Behavioral model that **focuses on modeling built-in offset of the AFE components and ISI from the channel**
- **Provides controllability over all AFE offset and channel coefficients** which can be **randomized in UVM-based testbench**
- Channel is implemented as a FIR filter which has 10 tap coefficients
- AFE offset is applied to the received data when it pass through each AFE component
- Magnitude of the **AFE offset and ISI can be mathematically calculated**




## PROPOSED METHODOLOGY

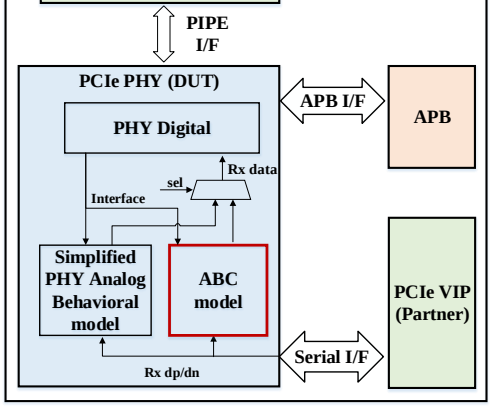
### Proposed UVM Testbench Architecture

- Integrate the ABC model with a Simplified Behavioral model that doesn't have AFE offset and channel characteristics
- Test cases that need Rx data reflecting AFE offset and ISI will only select the ABC model branch of the multiplexer

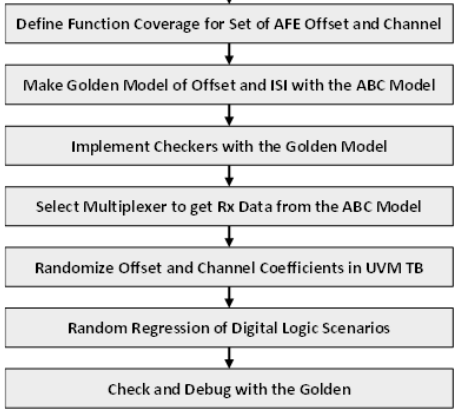
### Application of Proposed Methodology

- Applied to 16GT/s PCIe IP
- Rx digital logic including **EOM, Offset Calibration, DFE Adaptation, Rx Margin** was verified with ABC model
- Checkers are implemented based on the parameters of the ABC model
- **Found bugs that cannot be detected with a conventional analog behavioral model** that reflects the actual circuit

<UVM TB ARCHITECTURE>




<VERIFICATION FLOW>




## RESULTS

### Experimental Result

- Comparison performed on the **verification period of Rx digital logic**
- Conventional methodology used Xmodel for the analog behavioral model
- Code coverage closure : **70.3% reduced**
- Function coverage closure : 68.3% reduced

| | Verification Period (Hour) | | |
|---|---|---|---|
| | Conventional | Proposed | Reduction Rate |
| Average Sim Time | 6.53 | 2.01 | 69.2% |
| Time to achieve CC 100% | 54.26 | 16.13 | 70.3% |
| Time to achieve FC 100% | 106.75 | 33.87 | 68.3% |

## CONCLUSIONS

- Verification methodology for digital logic in mixed signal design is proposed
- ABC model ensures fast **debugging and high accuracy** in digital logic verification
- **Average simulation time of digital logic reduced by 69.2%** and achieved fast DV closure
- Additional enhancements in verification period are expected, considering the **time saved in configuring various AFE and channel environments and reduced debugging time**
- Can be effective except in cases where verification with the real analog circuit is necessary

## REFERENCES

[1] Mariam Maurice, "Functional Verification of Analog Devices modeled using SV-RNM" DVCON US, 2023

[2] Xmodel - "xmodel: Empower SystemVerilog with Event-Driven Analog Models," 2023. Available: https://www.scianalog.com/xmodel/

SAMSUNG

Samsung Electronics Co., LTD., Yongin-si, Korea

Contact Info : ky12.shim@samsung.com