A Hybrid Verification Approach for Cache Coherent Systems: Functionality and Performance

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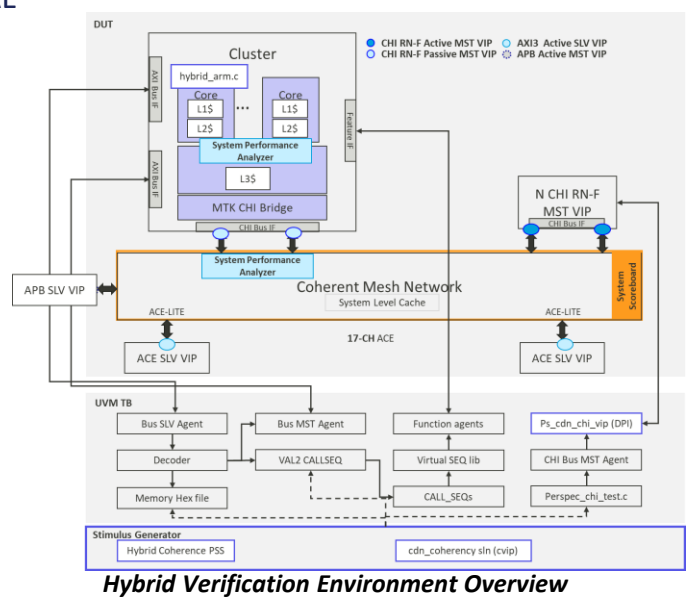
accellera SYSTEMS INITIATIVE

2025 DESIGN AND VERIFICATION™ DVCON CONFERENCE AND EXHIBITION UNITED STATES
SAN JOSE, CA, USA
FEBRUARY 24-27, 2025

VERIFICATION GOAL

Cache coherent systems are critical but challenging to verify:
- Lack of meaningful stimulus to test the cache protocol
- Need for a system coherent checker to guard functionality
- Need for a systematic methodology to evaluate system performance

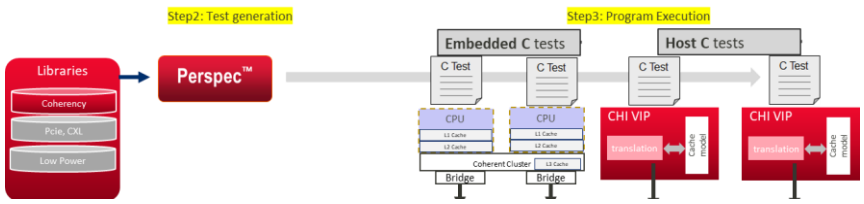
Proposes a comprehensive verification approach:
- **Perspec-built cache coherent library** generates C tests for snoop operations
- **CHI VIP's protocol coverage** reviewed for verification strength
- Custom CHI UVM sequence tested for **system performance**
- **System Verification Scoreboard** ensures cache coherency correctness
- **System Performance Analyzer** measures bandwidth and latency



Hybrid Verification Environment Overview

PROPOSED METHODOLOGY (1)

Proposed Verification Flow
1. Stress cache coherent stimulus generation for function
   - **Supports 9 scenario groups** of cache coherency
2. System verification scoreboard connected to guard cache protocol
3. System performance analysis to evaluate if there is a performance drop
4. CHI functional coverage development to ensure the quality of test regression



Cache coherent stimulus generation flow

PROPOSED METHODOLOGY (2)

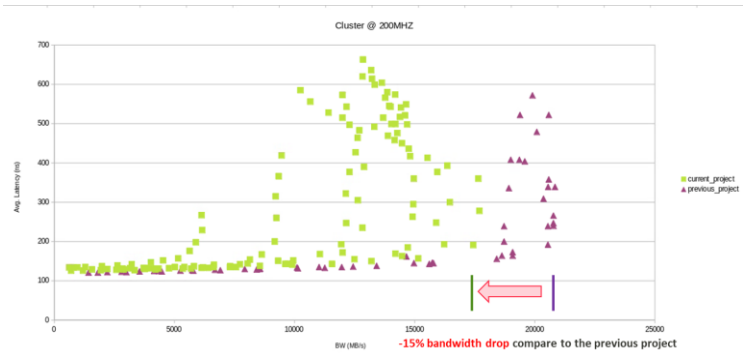
Performance Verification Flow
1. Developed for the **CHI VIP L3 cache read-hit sequence**
2. Recorded as input for the System Performance Analyzer
3. **Analyzes bandwidth of test scenarios** between the projects

Trend graphs of CHI VIP bandwidth

RESULT

- Identifying corner RTL issues related to **incorrect system cache line state** that cause system bus fabric hang.

- Finding a **15% performance drop** due to incorrect micro-architecture design.



Identification of bandwidth performance drop

CONCLUSION

1. Describe how the hybrid environment verifies the cache coherency system between cores and CHI-VIP by utilizing Perspec.
2. Introduce the system performance analyzer to obtain the performance raw data for comparison.
3. Collect functional coverage to prove the quality of verification.

CATEGORY	EXPECTED	UNCOVERED	COVERED	PERCENT
Variables	1468	235	1233	83.99
Crosses	5380	536	4844	90.04

Source File(s) :
/mtklib/soft/vent/Cadence/11.30.094-20231220/tools.lnx86/denali_64bit/ddvapi/sv/coverage/chi/denaliChiCoverage.svh

12 Instances:

NAME	SCORE	WEIGHT	GOAL	AT LEAST	AUTO BIN MAX	PRINT MISSING
uvm_test_top.infratba_test.env.CHI_RN_MST_MP0.monitor.coverModel.ItemEndedCover	85.73	1	100	1	64	64
uvm_test_top.infratba_test.env.CHI_RN_MST_MP1.monitor.coverModel.ItemEndedCover	86.99	1	100	1	64	64
uvm_test_top.infratba_test.env.CHI_RN_MST_MP2.monitor.coverModel.ItemEndedCover	86.51	1	100	1	64	64
uvm_test_top.infratba_test.env.CHI_RN_MST_MP3.monitor.coverModel.ItemEndedCover	86.62	1	100	1	64	64
uvm_test_top.infratba_test.env.CHI_RN_SLV_CMN0.monitor.coverModel.ItemEndedCover	79.81	1	100	1	64	64
uvm_test_top.infratba_test.env.CHI_RN_SLV_CMN1.monitor.coverModel.ItemEndedCover	75.34	1	100	1	64	64
uvm_test_top.infratba_test.env.CHI_RN_SLV_CMN2.monitor.coverModel.ItemEndedCover	80.33	1	100	1	64	64
uvm_test_top.infratba_test.env.CHI_RN_SLV_CMN3.monitor.coverModel.ItemEndedCover	79.99	1	100	1	64	64
uvm_test_top.infratba_test.env.CHI_RN_SLV_CMN4.monitor.coverModel.ItemEndedCover	82.30	1	100	1	64	64
uvm_test_top.infratba_test.env.CHI_RN_SLV_CMN5.monitor.coverModel.ItemEndedCover	74.62	1	100	1	64	64
uvm_test_top.infratba_test.env.CHI_RN_SLV_CMN6.monitor.coverModel.ItemEndedCover	81.15	1	100	1	64	64
uvm_test_top.infratba_test.env.CHI_RN_SLV_CMN7.monitor.coverModel.ItemEndedCover	77.13	1	100	1	64	64

Variables for Group Instance uvm_test_top.infratba_test.env.CHI_RN_SLV_CMN0.monito

VARIABLE	EXPECTED	UNCOVERED	COVERED
QoS	16	0	1
ReqOpCode	70	0	7
WriteDataOpCode	6	1	
CompDataOpCode	2	0	
CompOpCode	4	2	
Size	7	0	
TagOp	4	0	
NonSecure	2	0	
NonSecureExt	2	1	
StashNIDValid	2	0	
StashLPIDValid	2	0	
Endian	2	0	
Deep	2	0	
LikelyShared	2	0	
Order	3	0	
MemAttr	6	0	
SnpAttr	2	0	
DvmDomain	2	0	

83% single coverpoints and 90% cross coverpoints of the CHI interface protocol

ACKNOWLEDGMENTS

For any further details, please send an email to the following address: Jiang-Tang.Xiao@mediatek.com.