Enhancing SDC Verification in SoCs: Heatmap Visualization and Machine Learning Approaches for Optimal Coverage Closure

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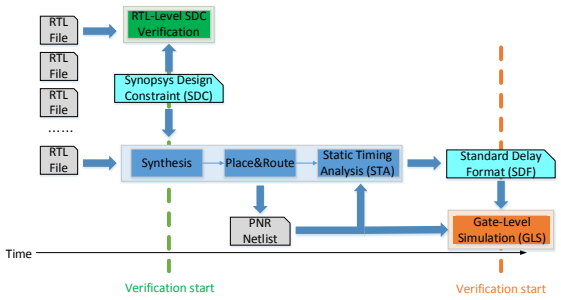
Introduction – SDC verification and Shift-Left

- Role of SDC: Defines timing constraints to meet PPA goals
- Importance of SDC Verification: Mismatches lead to performance loss or chip failures
- GLS Limitations: i) Starts late, ii) Slow & liming test coverage
- Shift-Left with SDC-Aware Simulation (RTL-level Verification): i) Early issue detection, ii) Reduces GLS dependency

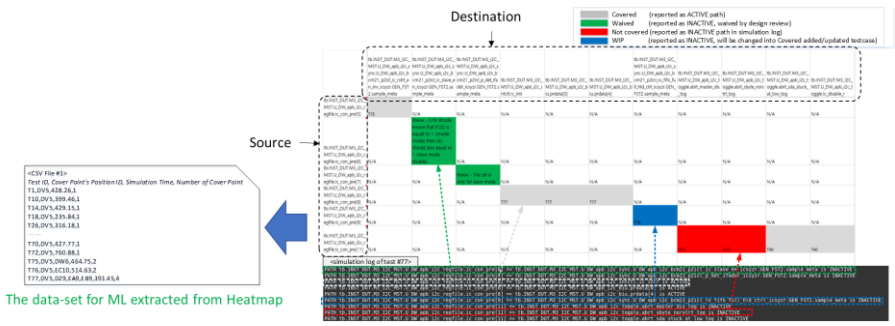


Remaining Challenges and Proposed Solutions

- Challenges with SDC-Aware Simulation
  - High review burden: Too many SDC errors & warnings
  - Long coverage closure TAT: Slow regression cycles
- Proposed Solutions
  - Heatmap visualization to focus review efforts
  - ML-based regression optimization to accelerate coverage closure

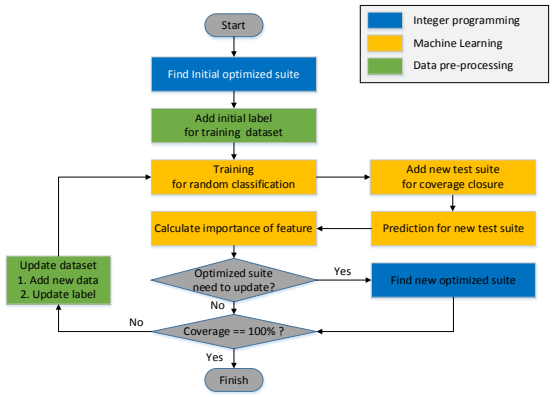
Approach 1 – Heatmap Visualization

- Intuitive Visualization: Easily identify SDC coverage gaps and track source-to-destination path based verification progress
- Data Foundation for ML: Structured coverage data enables ML-driven test optimization



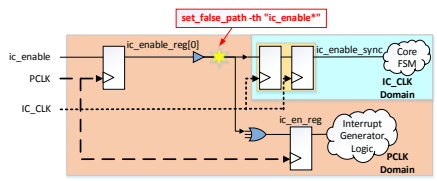
Approach 2 – Optimization Problem and ML

- Smarter Test Selection: ML prioritize high-impact tests, reducing regression time
- Faster Coverage Closure: Eliminates redundant tests while ensuring full verification



Early Detection of SDC Errors

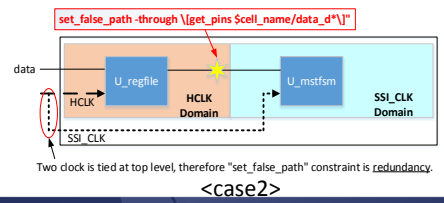
- Prevents costly design iterations by catching incorrect SDC early
- Filters redundant constraints, reducing verification debug and manual review effort



<case1>

Case 1: Incorrectly defined constraints

- Misaligned timing exceptions due to misunderstood clock relationships
- Causes functional issues, requiring SDC or design updates



<case2>

Case 2: Redundant constraints

- Unnecessary false paths due to incorrect assumptions at the top level
- Can be waived after architectural review to reduce verification workaround

Results and Conclusion

- Experiment Results
  - Regression test suite size reduced (target IP with 387 timing exception path): 78 → 19 tests
  - Verification runtime reduced: 27 → 10 hours
  - Improved GLS verification: A optimized test vector now covers 60% of SDC paths (vs. 0.3% before)

	Existing method	Proposed approach
Regression suite size	78 test vectors	19 test vectors
Regression Turn-Around-Time (TAT)	27 hours	10 hours

- Conclusion
  - Proposed methodology enhances SDC coverage while reducing regression time by 63%
  - Heatmap visualization and ML-driven optimization minimize manual effort and accelerate verification cycle
  - Future work: Scalability challenges remain for larger designs

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