A Statistical and Model-Driven Approach for Comprehensive Fault Propagation Analysis of RISC-V Variants

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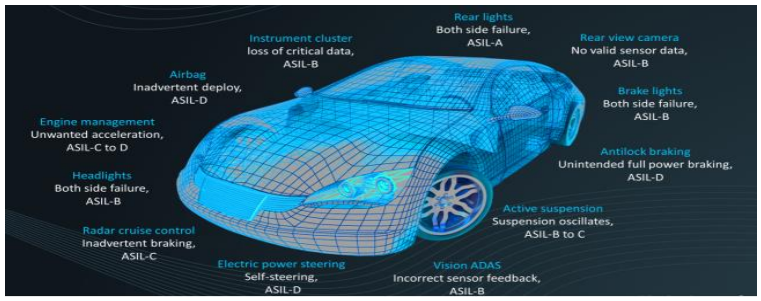
INTRODUCTION

Growth of digital design complexity

44% of ASIC projects have integrated safety-critical features

Verification of safety-critical designs remains a bottleneck

Huge number of stuck-at fault locations in designs



OBJECTIVES

Safety-critical designs require fast, accurate and automated verification techniques

Statistical and probabilistic approach required to analyze numerous faults in the design

This work intends to improve the overall safety analysis process

- Increase automation, performance, and productivity
- Reduce efforts of fault injection process

Automation is achieved through metamodeling

STATISTICAL FAULT INJECTION

The amount of *n* faults to inject

- Initial population size N
- Standard error p
- Margin of error e
- Confidence level Z parameter

$$n = \frac{N}{1 + e^2 \times \frac{N-1}{z^2 \times p \times (1-p)}}$$

When N is very large:

- $n = \lim_{N \to \infty} f(N) = \frac{z^2}{e^2} \times p \times (1-p)$

	95 % confidence z = 1.96	99% confidence z = 2.5758	99.8% confidence z = 3.0902
e = 5%	n =384	n= 663	n= 955
e = 1%	n = 9581	n= 16519	n= 23874

APPLICATION

SFI on two distinct RISC-V-based RV32-IMC CPU subsystems

Fault injection performed on different CPU modules

- Arithmetic-Logic Unit (ALU)
- Instruction Decoder
- Branch Control Unit (BCU)

SFI process: 5% error margin and varying confidence rate: 95%, 99% and 99.8%

Four distinctive benchmarks: Dhrystone, SHA-256, MD5, CRC-32

RESULTS

Fault propagation on 2-stage CPU using Dhrystone benchmark

	99.8%	99%	95%
ALU	40.1	42.2	40.6
Decoder	48.4	50.2	50.8
BCU	31.3	30.9	34.6

Fault propagation on 2-stage CPU using SHA-256

	99,8%	99%	95%
ALU	42.7	44.8	44.5
Decoder	47.0	48.3	47.9
BCU	25.6	25.0	25.8

CONCLUSIONS

This work introduced statistical analysis and model-driven techniques to evaluate the Fault Propagation Analysis of different versions of RISC-V processor

Two separate RISC-V CPU subsystems were employed, and each was subjected to multiple trials utilizing four diverse workloads (benchmarks)

Fault propagation consistently remained within a margin of error range of 5% regardless of the varying confidence rates applied

Future work: comparisons and assessments with other fault simulation tools