# Innovative 4-State Logic Emulation for Power-aware Verification

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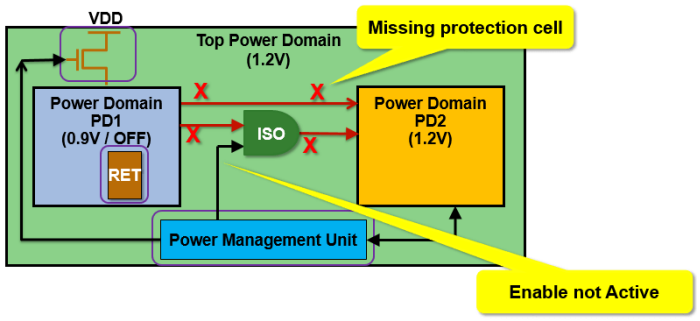
## BACKGROUND

- Power aware verification including UPF is always a long pole in SOC projects.
- Traditional emulation supports only 2-state logic ('0' and '1'). 'X' and 'Z' are not supported.
- We might miss power intent bugs.




## 4-STATE LOGIC EMULATION

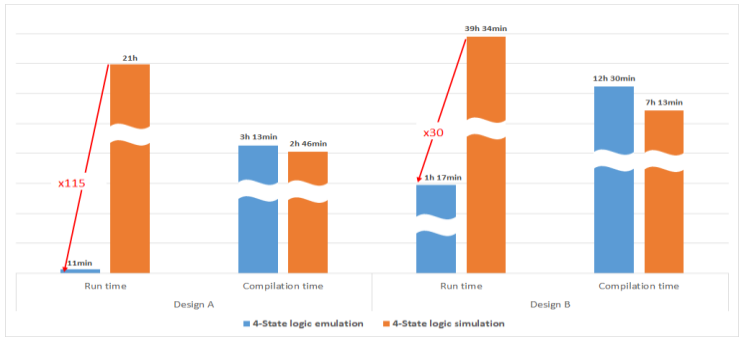
- With the novel implementation of native 3-state ('0', '1', 'X') computation in the Palladium Z2 processor along with additional compiler logic transformations to add 'Z' support
- 4-state hardware emulation is now practical to implement and well suited for low-power verification
- The usage methodology for 4-state emulation retains the same features, compile flow and run-time operation as 2-state emulation
- The emulation resources required for 4-state calculations must be at least two times that of 2-state calculations

## Requirements for successful 4-State logic emulation

- Power aware synthesizable (for emulation) PHY model: All power features including power pins and the model should be working with UPF at the same level as the simulation model
- Removal of Dynamic RTL(emulation debug feature) : dynamic RTL is not supported with 4-State emulation
- PAD MUX implementation for taking care of high 'Z' and 'X' values
- Handling pull-up/pull-down for 'Z' state net
- SRAM/ROM code preloading : preload to avoid unexpected 'X' propagation after accessing an un-initialized memory region

## RESULTS – Runtime / Compilation time

- Runtime : 30~115 times faster than simulation, depending on design size and test scenario.
- Compilation time : 1.16~1.7 times longer than that of the simulator.




## Resource Analysis

- 'Emulation capacity' refers to the volume of resources utilized by the emulator hardware
- 4-State emulation requires approximately 2.3 times more resources than 2-State emulation
- Adding UPF increases overall resource usage by approximately 3.2 times compared to the default configuration.

| Mode | Relative Cost | 2-State w/o UPF | 2-State w/ UPF | 4-State w/o UPF | 4-State w/ UPF |
|---|---|---|---|---|---|
| Emulation capacity | vs. 2-State | 1 | 1.4x | 2.3x | 3.2x |
| | vs. 2-State w/ UPF | | 1 | | 2.3x |
| Compile time | vs. 2-State | 1 | 1.5x | 1.5x | 2.1x |
| | vs. 2-State w/ UPF | | 1 | | 1.4x |
| Performance | vs. 2-State | 1 | 0.75x | 0.9x | 0.59x |
| | vs. 2-State w/ UPF | | 1 | | 0.81x |

## CONCLUSIONS

- This paper introduces the innovative 4-State logic emulation technology for power-aware verification and presents the evaluation result through an actual mobile-AP SOC project for the first time in the verification industry
- The 4-State emulation is highly useful for identifying power intent bugs, such as missing isolation cells, and makes it simplifies the debugging of 'X' sources
- Experimental results reveal that 4-State emulation is significantly faster than simulation, approximately 30~115 times faster, depending on design size and scenario complexity

## Acknowledgment and Contact Information

- We would like to express our appreciation to our team members who assisted with the debugging, especially in finding the 'X' root causes, and to the PHY modeling team who implemented the synthesizable emulation PHY models.
- We would also like to thank the Cadence members who collaborated to enable this methodology.
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