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Automating Datapath Verification and Bug Correction via Equality Saturation

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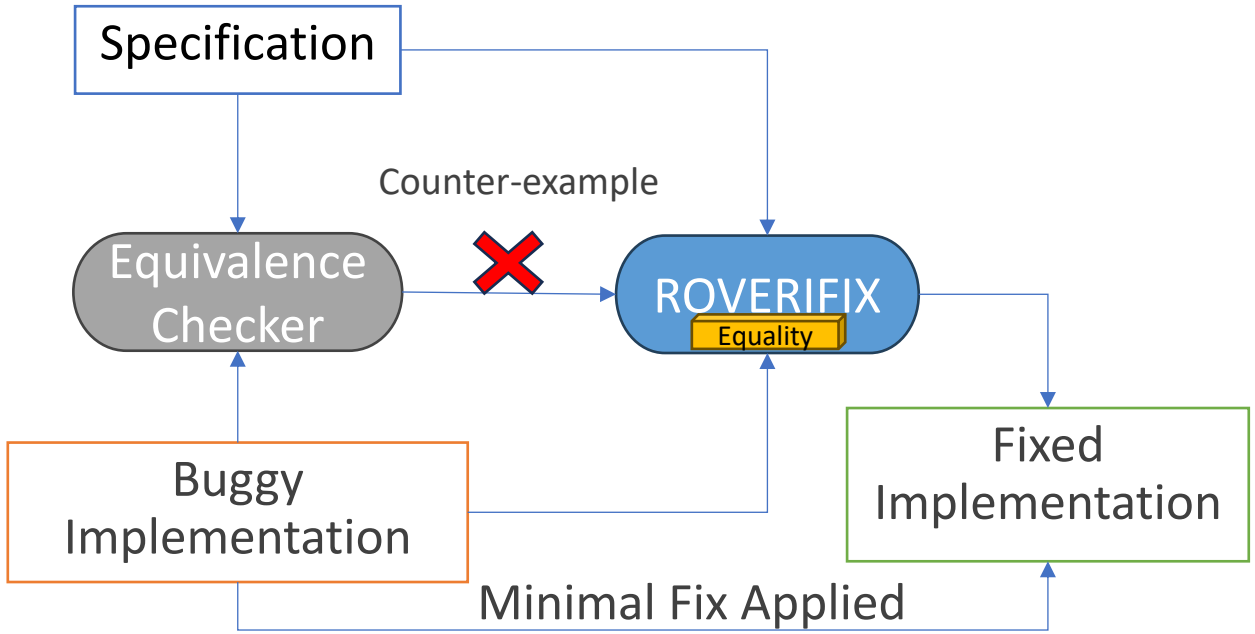
Intel and Imperial College London

intel IMPERIAL

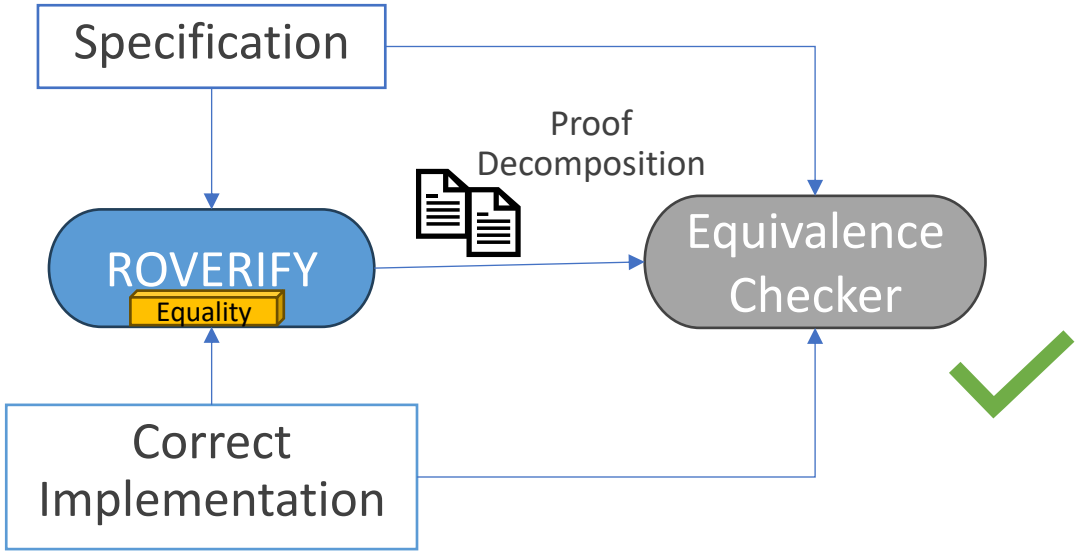
accellera SYSTEMS INITIATIVE

Datapath Debug and Verification

Core RTL Equality Saturation Engine



Automatically correct datapath bugs



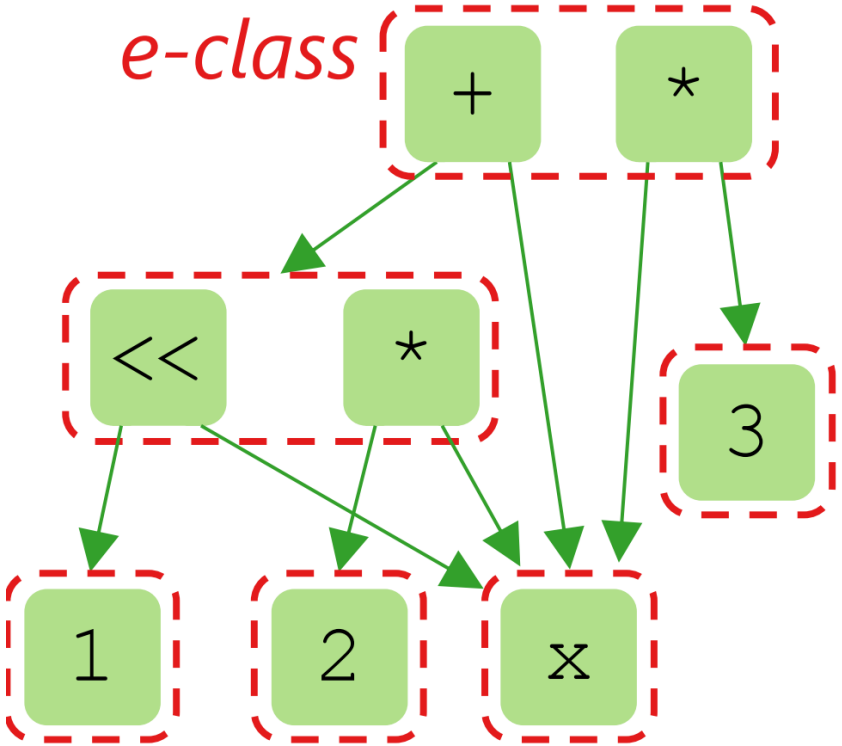
Automatically decompose datapath equivalence proof

Equality Saturation

Egg Rust
E-graph Library

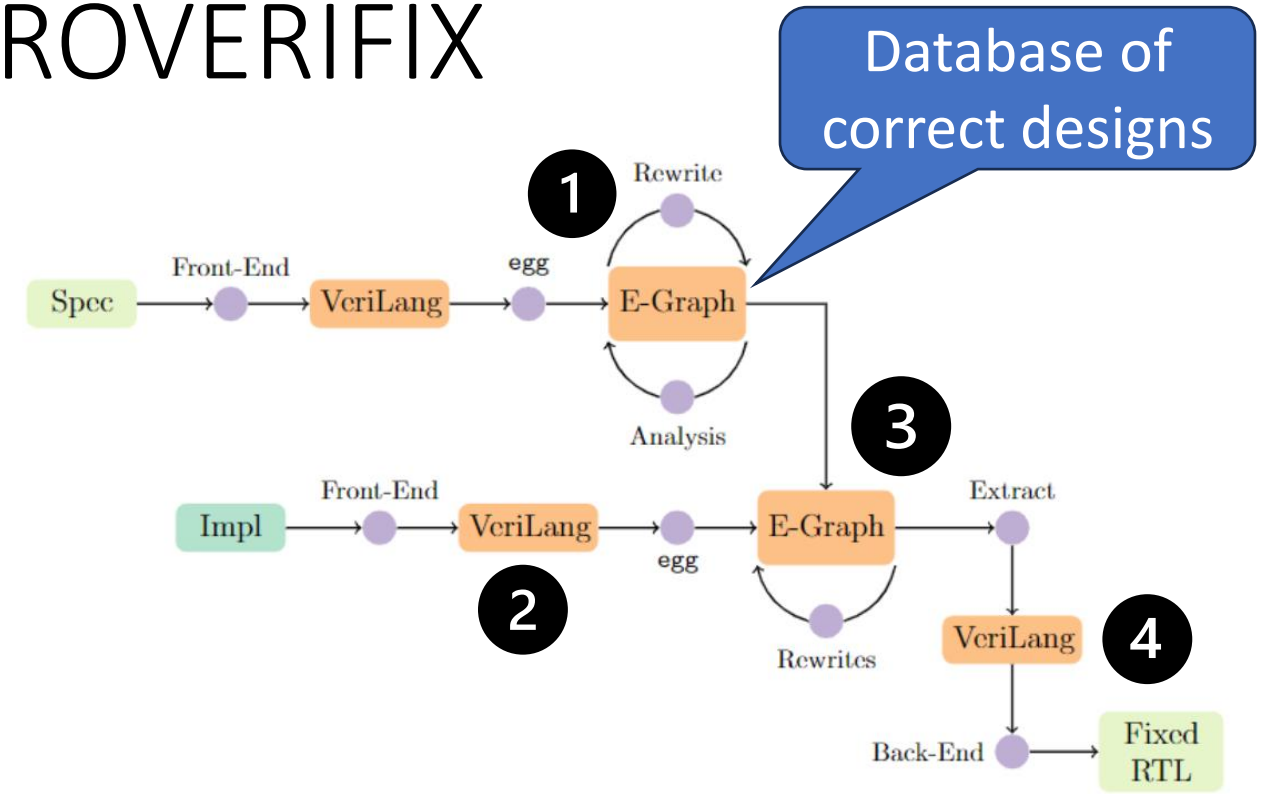
$$\underbrace{(x \ll 1)}_{(x * 2)} + x$$

$$x * 3$$



- Represent RTL designs as an e-graph
- Discover equivalent designs via constructive rewriting
- Maintain complete history

ROVERIFIX



1. Initialize Spec e-graph – apply datapath rewrites
2. Insert FIX(spec, impl) into e-graph
3. Propagate FIX operators to isolate the bug
4. Extract the design closest to impl that is equivalent to spec

Datapath Rewrite Examples:

- $a \ll (b + c) \rightarrow (a \ll b) \ll c$
- $a \times (b \ll c) \rightarrow (a \times b) \ll c$

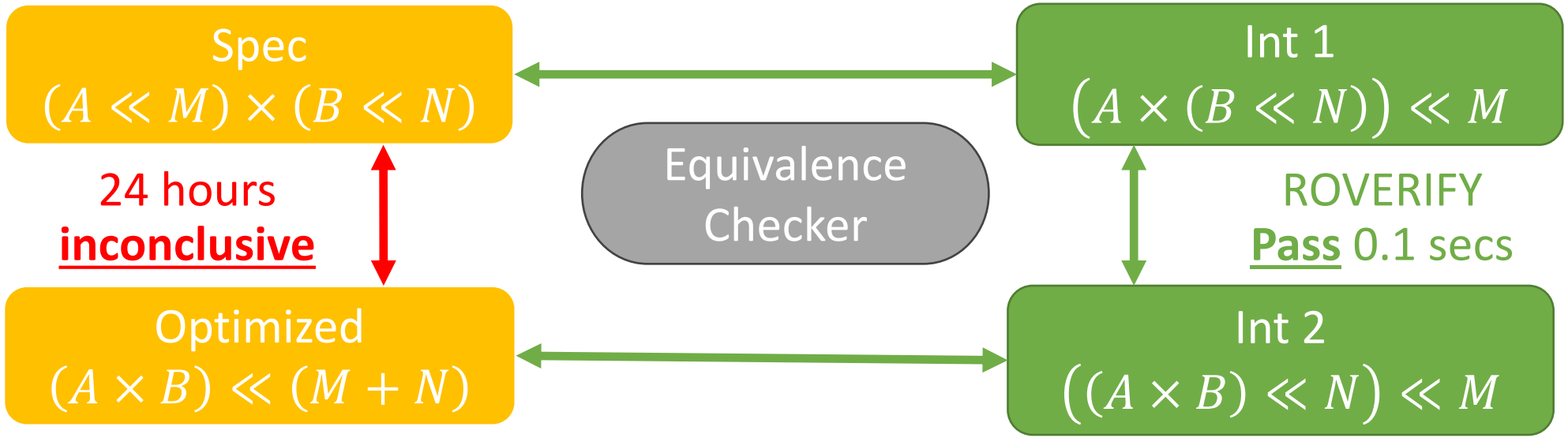
Results

Fix automatically generated by ROVERIFIX

```
1   module spec(A,B,C,out);
2   input  logic [7:0] A, B, C;
3   output logic [9:0] out;
4   wire  [8:0] add_right;
5
6   assign add_right = B + C;
7   assign out       = A + add_right;
```

```
1   module impl(A,B,C,out);
2   input  logic [7:0] A, B, C;
3   output logic [9:0] out;
4   wire  [7:0] add_8bit;
5
6   assign add_8bit  = A + B; // carry-out discarded
7   assign out       = add_8bit + C;
```

Proof automatically decomposed by ROVERIFY



Average **2.8x speedup** in proof time across datapath benchmarks