SYNOPSYS®

Re-Engineering Engineering

For AI Chip Design, Verification and Optimization

Vikas Gautam, VP Engineering

DVCON India, September 2025

Legal Disclosure

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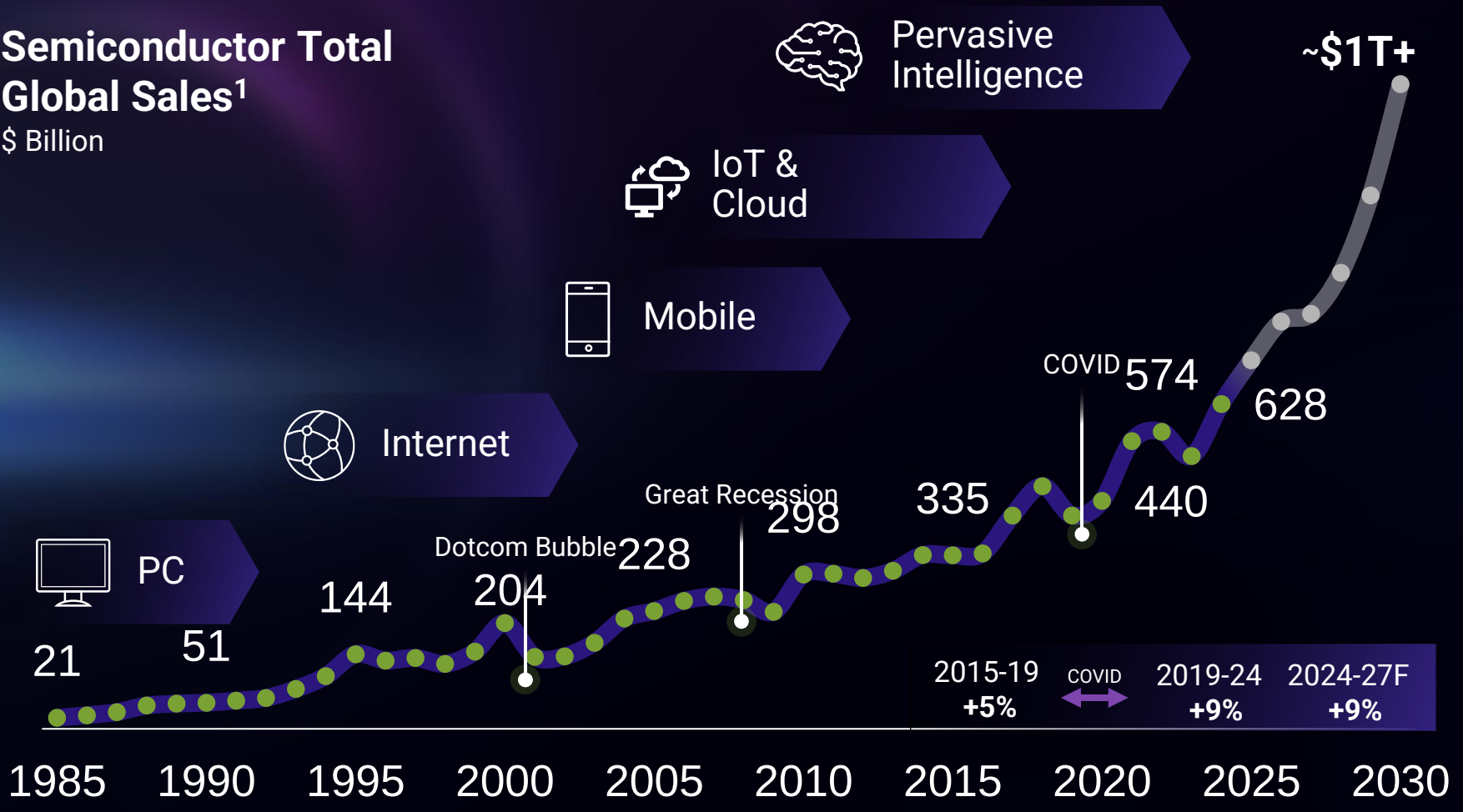
Agenda

- Industry Trends
- 2024 Recap and More Challenges Emerge
- Technology Evolution by Example – Microsoft
- Use Cases
  - Driving Reconfigurability & Modularity
  - EP=Ready Hardware
  - Driving Verification Requirements
- AI for Productivity Improvements
- Outlook: Where do we go from here?

A new era of semi demand acceleration

Semiconductor Total Global Sales[1]
$ Billion



Explosion in demand for AI chips[2]

Potential **$500B+** (~30% CAGR) in xPU revenues by 2029

1. Sources: WSTS (actuals); Forecasts based on WSTS, Gartner, Tech Insights, IBS, Semi Sample
2. Sources: New Street Research, AMD, Nvidia, TSMC, Intel, Goldman Sachs

Impact of the latest AI trends

Energy

4GW

powered data centers

Source: Tech Crunch, Meta

AI Models

50T

50 trillion tokens per month

Source: Microsoft Azure, 2025

Agents

$155B

agentic spending by 2030

Source: Bank of America, 2025

Economy

15%

boost to global GDP by 2035

Source: PWC, 2025

Recap from Last Year’s Discussion

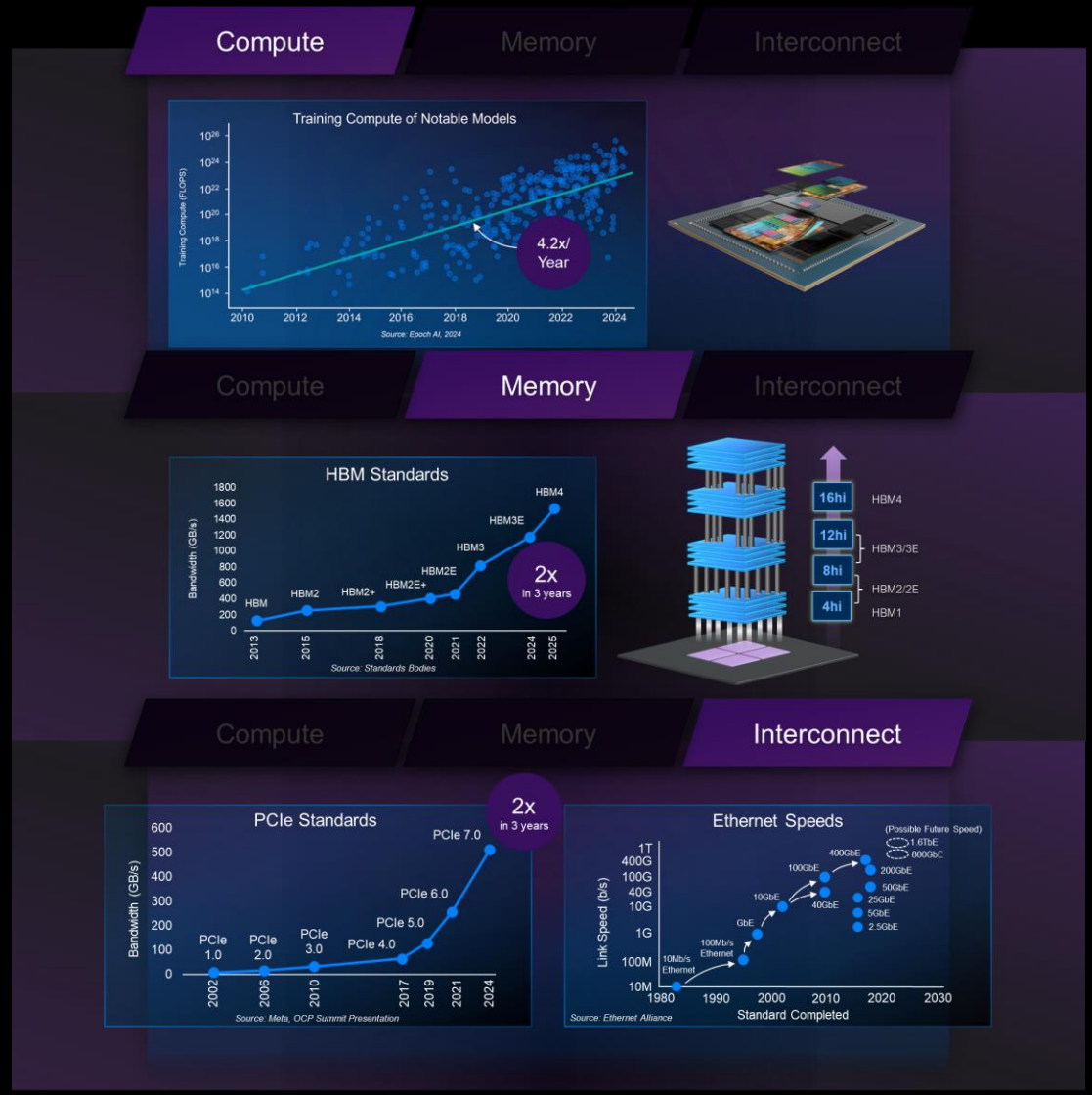
Google & Synopsys

Recap from Last Year: AI & Google

Three Drivers: Compute, Memory and Interconnect

Era of Pervasive Intelligence

Semiconductors Appear Everywhere

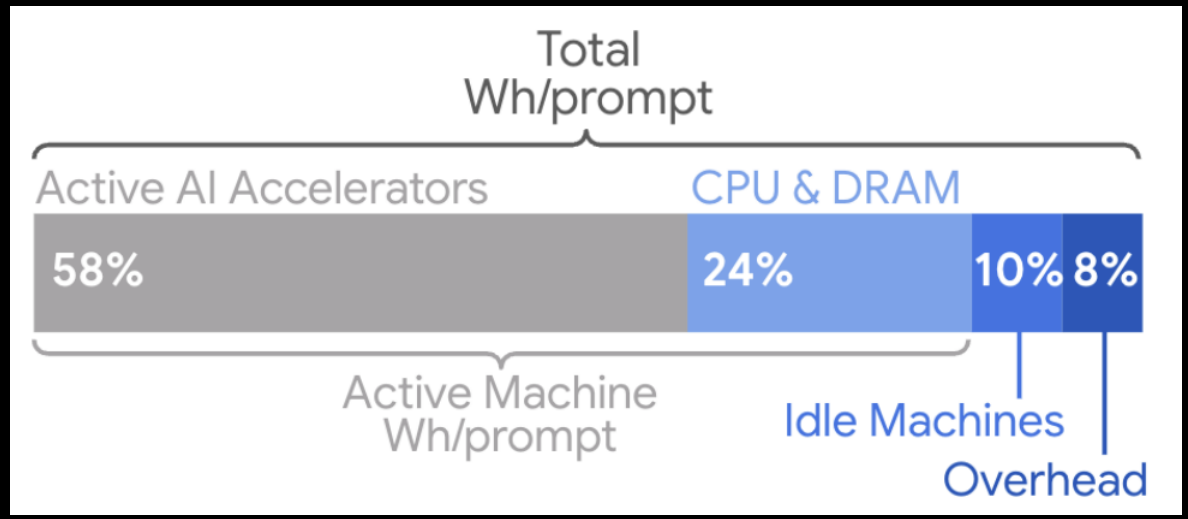


And The Challenges Only Grow!

And Accelerated Low Power Demands from Datacenters

Gemini Text Prompt: 9 seconds of watching TV …

The median Gemini Apps text prompt uses ***0.24 watt-hours (Wh) of energy, emits 0.03 grams of carbon dioxide equivalent (gCO2e), and consumes 0.26 milliliters (or about five drops) of water*** *— figures that are substantially lower than many public estimates. The per-prompt energy impact is e****quivalent to watching TV for less than nine seconds****.*



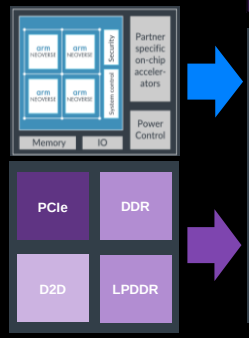
Source: How much energy does Google's AI use? We did the math

AI Workloads Drive Datacenter-level Optimization & Verification

From compute and interface IP to running AI workloads

arm

Neoverse CSS



Interface IP

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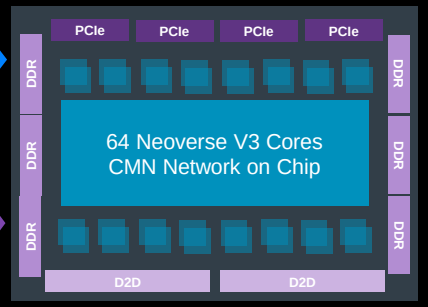
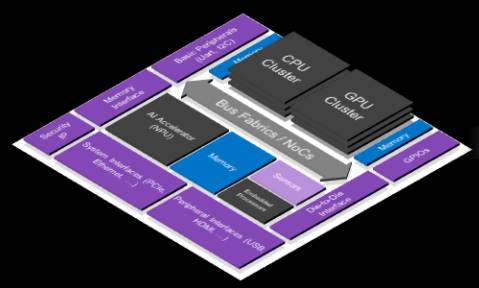
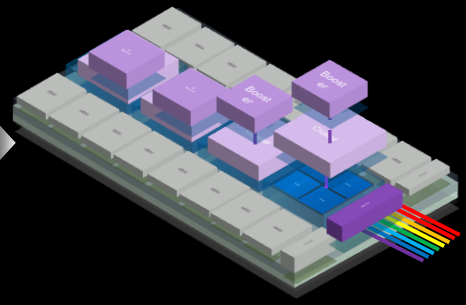


Compute Sub-system

Applications
Middleware
OS
Drivers



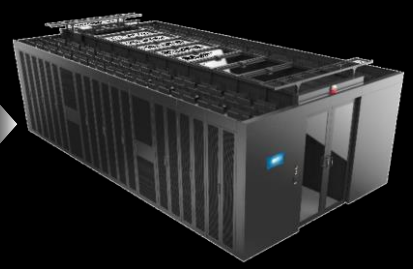
Silicon Architecture



Advanced Packaging

Models & Applications
AI Frameworks (e.g., PyTorch, ONNX Runtime)
HW Abstractions & APIs (CUDA, ROCm, MAIA, …)

Scale-Up



Scale-Out

NoC configuration?

How to get to lowest power?

What is the best Chiplet partitioning?

Workload-specific AI/Compute architectures?

How to ensure reliability throughout lifecycle?

How to get 17% more performance?

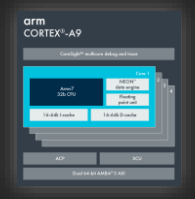
Validate AI Workloads on IP and SoC?

How to validate cache coherency?

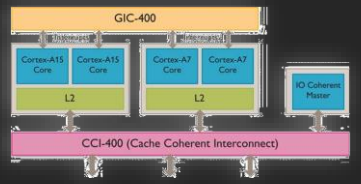
Accelerating IP Re-use at Higher Hardware/Software Complexity

1998
Arm 9

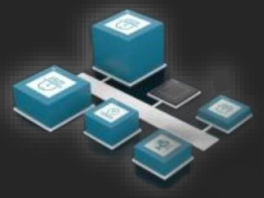
2007
Arm Cortex A9



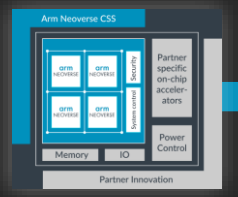
2011
BigLITTLE



2017
Arm DynamiQ

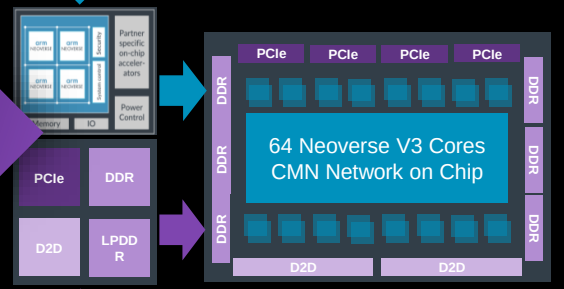


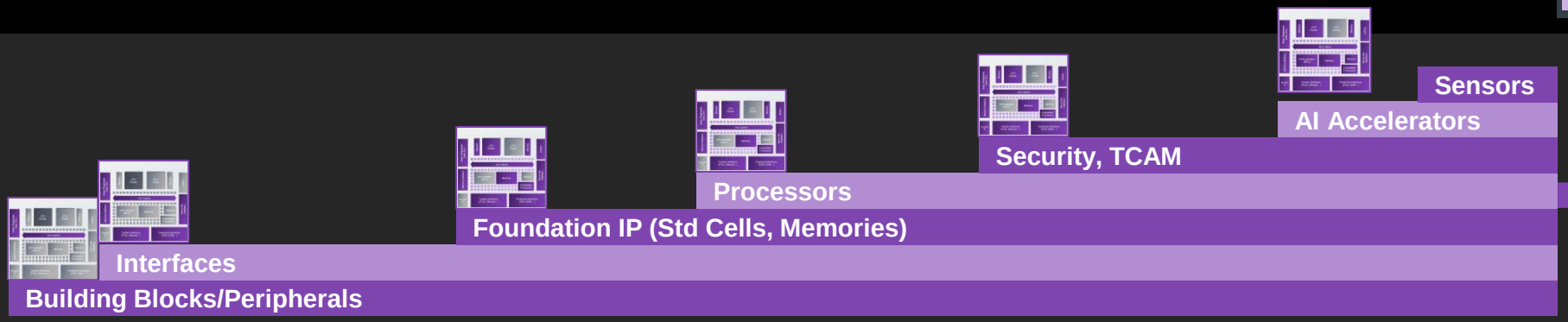
2023
Arm CSS N2



arm

Core → Multicore → Multi-die





2000 2010 2020

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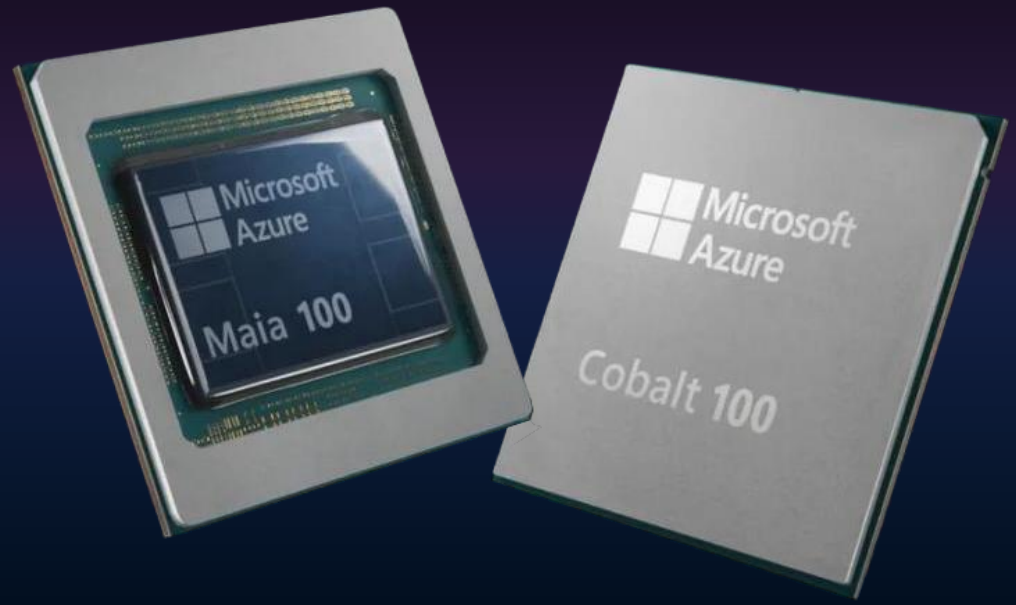
Technology Evolution by Example

Microsoft & Synopsys at DVCON US 2025

The KPI for the World's Computer and AI Factories

Performance / $
Performance / Watt

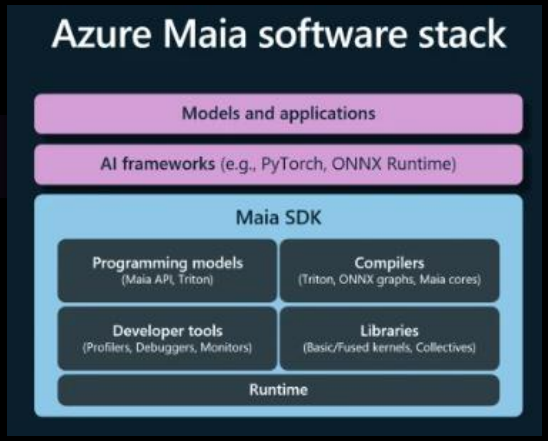


Microsoft

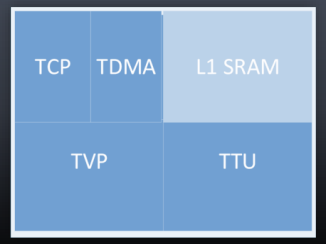
Use Cases are Driven by AI Workloads

Application of AI Workloads needs to shift left as far as possible

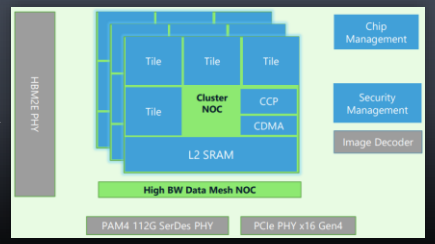
WORKLOADS



Silicon IP / Blocks

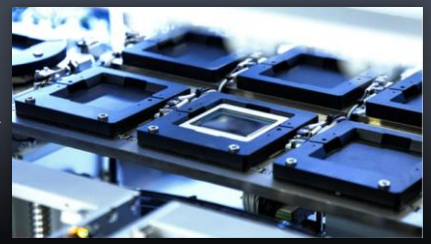


Architecture

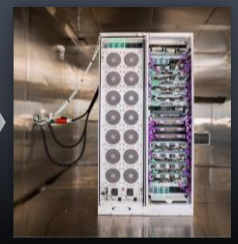


Silicon

Silicon in Board

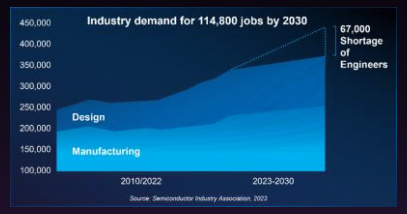


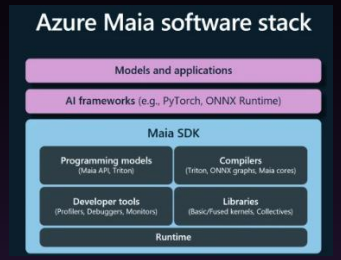
Systems

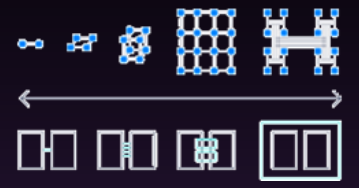


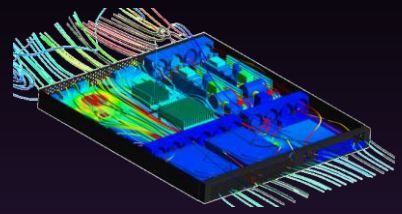
Many Use Cases: IP in System Validation, Performance Validation, Compliance, Functional Verification, RTL Regressions, Early Software Bring-up, Hardware/Software Validation, Early Performance and Low Power Analysis, Reliability, Security, Design for Test, Silicon Lifecycle Management

Microsoft’s Asks to the Industry - Capabilities







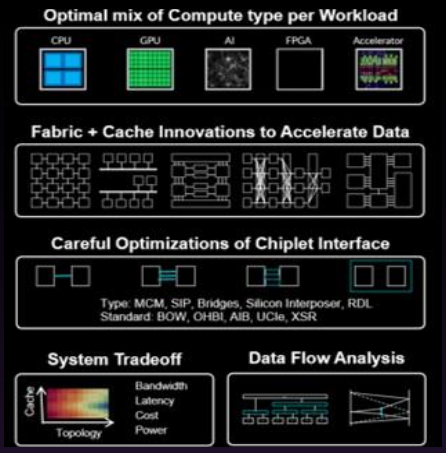


AI for Design	Early Software Workloads	Modular Approaches & Distributed Systems	Fabrics	End to End Thermal
Need 2x end-to-end efficiency in the next 2-3 years	Performance & Capacity of Engines	Brute force approaches become ineffective	High bandwidth Low power scalable configurable	Capabilities exist
We are just scratching the surface	Analysis and optimization	Multi-chiplet, Multi-SoC	Supporting multi-chiplet design	Not yet fully integrated into the silicon design Flow

Source: Microsoft, Synopsys, Baya Systems, ANSYS

Microsoft

Microsoft’s Asks to the Ecosystem



Industry Standards

Industry collaboration on standardization

System Interfaces

Rack formats and other components

Innovation & IP Reuse/Integration

Customization is justified if it significantly improves KPI

Source: Microsoft, Synopsys, Baya Systems

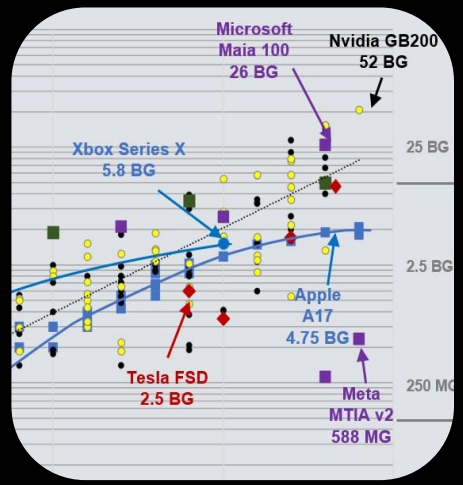
Microsoft

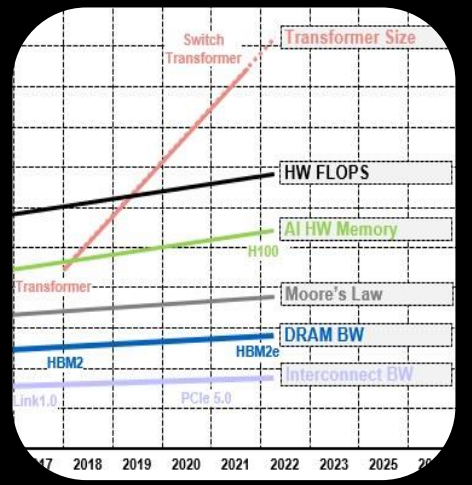
Use Cases Drive Reconfigurability & Modularity

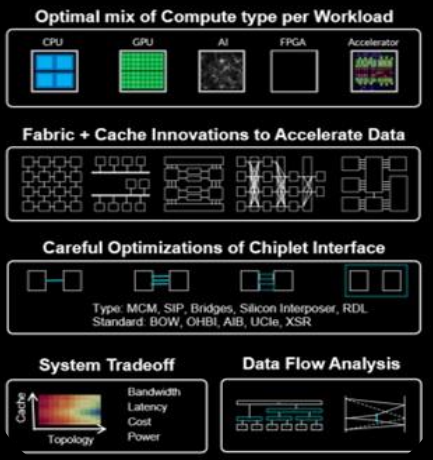
Compounding Complexities

Hardware-assisted Verification (HAV): The Keystone for Ensuring Functionality, Power and Performance

Software x **Hardware** x **Interfaces** x **Architectures**







Verification Challenge: **Quadrillions of Cycles***

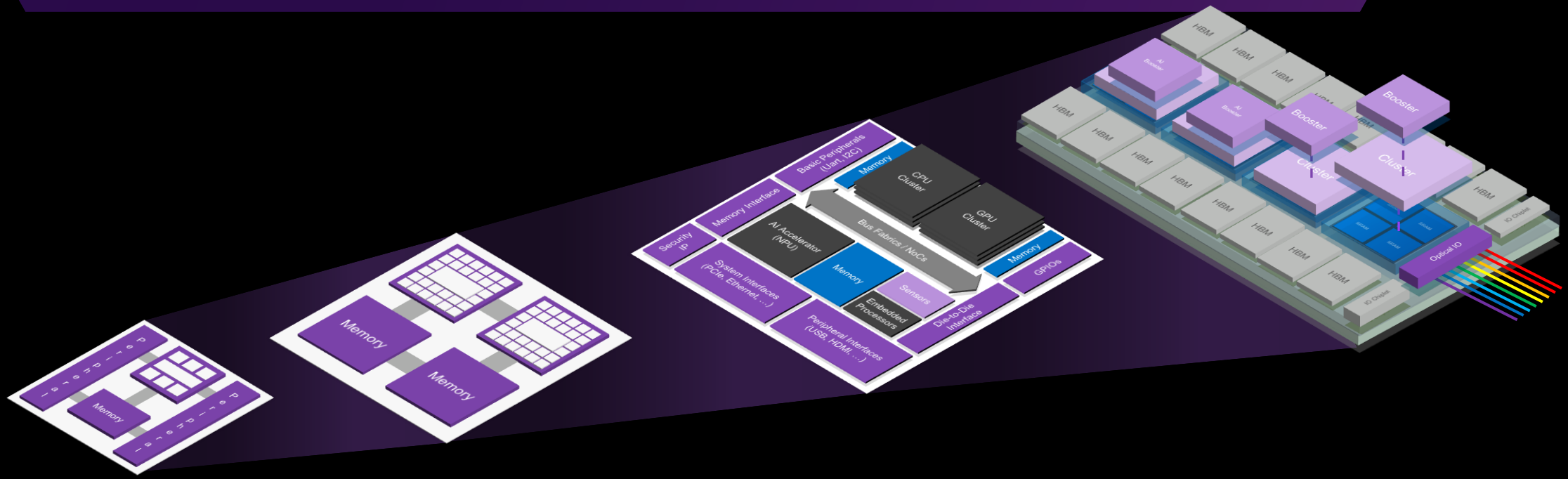
Sources: Synopsys, AI and Memory Wall: 2403.14123 (arxiv.org), Baya Systems, *"What Makes RISC-V Verification Unique?" https://bit.ly/4hDXCe9, Milad Fahmy, http://bit.ly/3UJGD03

Verification needs Quadrillions of Cycles!

From ISA Through CPU, Clusters of CPUs and Systems on Chips / of Chiplets

Simulation **Silicon**

Hardware-Assisted Verification



IP/Core Centric **Subsystem / Software** **Full Chip(let) / Software** **Multi-die / Software**

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Configurability for EP-Ready Hardware

Enabling Different Hardware/Software Stacks optimized for Emulation and Prototyping

up to **15.4 BG**

8x Debug

Faster Compile

Emulation Use Cases

ZeBu Software

Interfaces Memories

Cabling for **Design Flexibility**

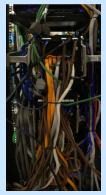
2x Performance

6 x AMD VP1902 Adaptive SoCs

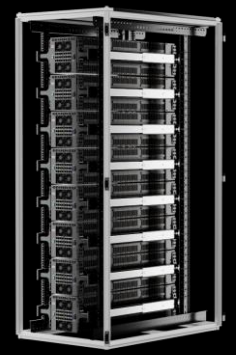
Prototyping Use Cases

HAPS ProtoCompiler

Interfaces Memories



Cabling for **Design Performance**



up to **10.8 BG**

4x Debug

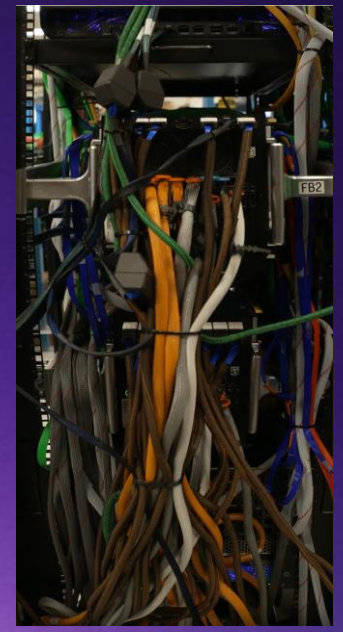
HAPS Ecosystem

Emulation Cabling for **Design Flexibility**

ZeBu Software **Emulation**

EP SW Transition

HAPS ProtoCompiler **Prototyping**



Prototyping Cabling for **Design Performance**

ZeBu-200

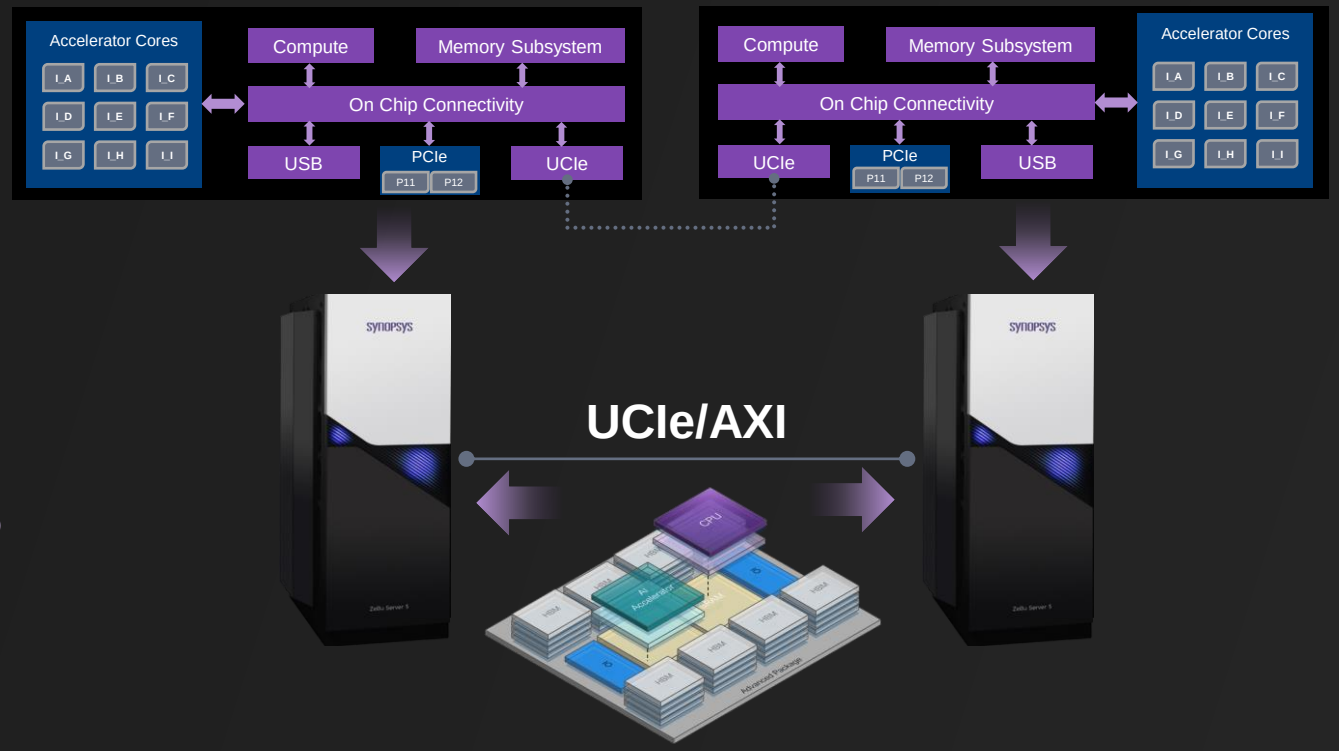
HAPS-200

SYNOPSYS®

Vision to future HPC/Data Center Needs

Modular Verification and Optimization for Sub-system Reuse

- Scale for **large multi-chiplet systems**
  - **Standard interfaces**
  - Reduces **time-to-model**
  - Extends **scalability** to beyond 60BG
- Arm CSS Integration
  - Pre-validated **integration with Synopsys IP**
  - Arm CSS-Ready Silicon to Systems Design
  - Save up to 80 man-years / 18 month



arm

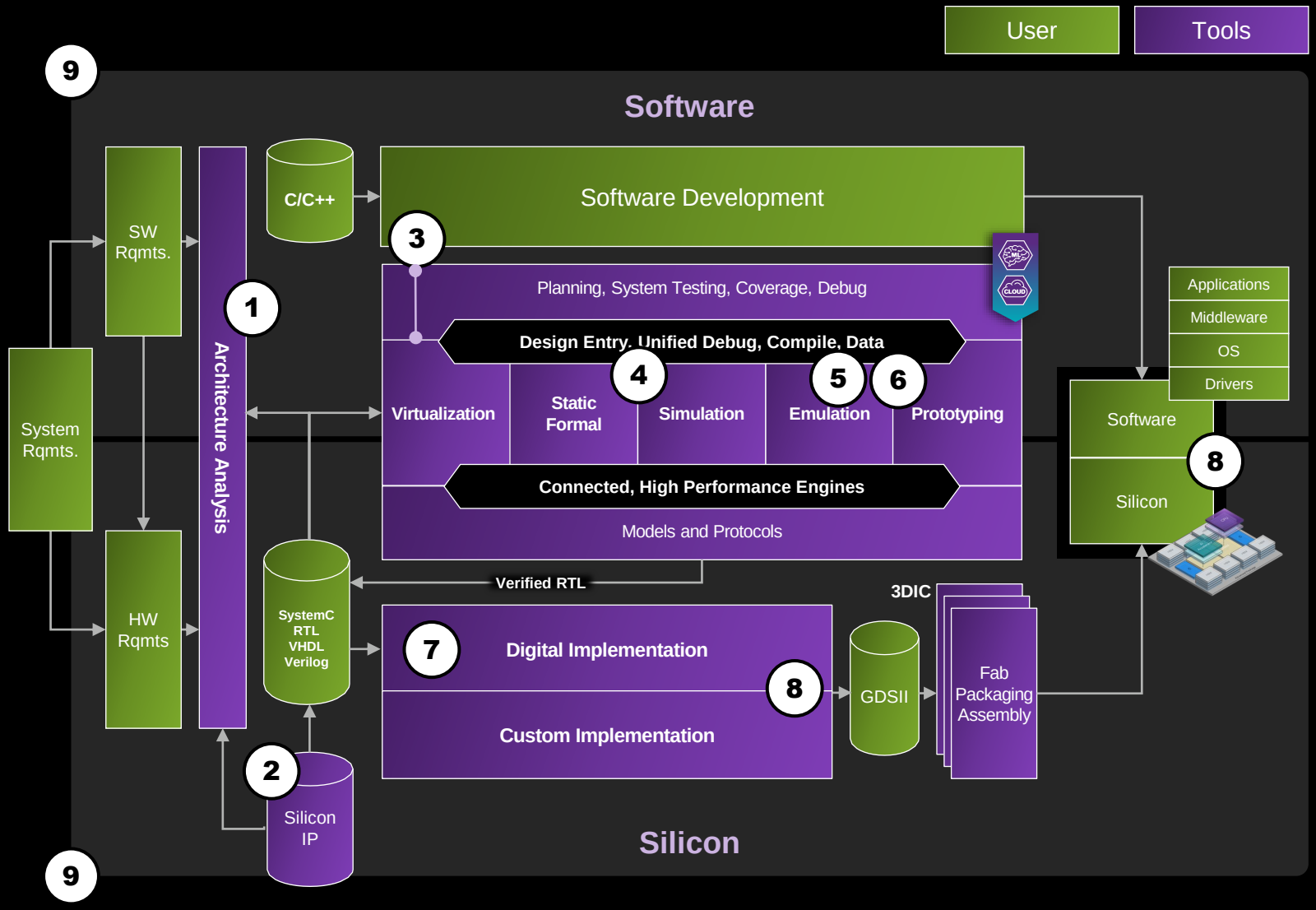
"Synopsys is a **key member of Arm Total Design**, bringing **critical tools and the advanced HAV capabilities** to quickly and **reliably validate** solutions built on **Arm Compute Subsystems** (CSS),"

Kevork Kechichian, Executive Vice President, Solutions Engineering, Arm

Putting it all together into a flow

A Silicon to Systems Design Flow

The North Star for Arm CSS Integration



1. Architecture Analysis for Arm CSS
2. Arm CSS-Ready IP Portfolio
3. Virtual Prototypes for Arm CSS SW Dev
4. Arm CSS/IP/VIP Integration Verification
5. Arm CSS in System V&V, Perf, Power
6. Arm CSS SW at high fidelity (Emu/Proto)
7. Arm CSS PPA Optimization
8. Silicon Lifecycle Management
9. Expertise & Services

Hardware-Assisted Verification Solutions

Use Cases from HW/SW through Verification to Compliance

Verdi & VCS

Early RTL Verification

Test	P/F
1	☑
2	☑
3	☒
4	☑

RTL Regression

Virtualizer

Software Bring-up

Highest Scalability
Best Density

Highest Performance
EP-Ready Hardware

Power/ Performance Analysis

ZeBu Empower

Platform Architect

Software/ Hardware Validation

HAPS Protocol Interface Card

Speed Adaptor

Compliance/ Certification

HAPS IP Prototyping Kit

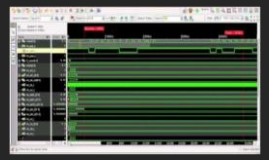
Unified Core Technologies: Compile, Debug, Hybrid, Transactors

Protocol Solutions for all Use Cases

PCIe, CXL, USB, HBM, UCIe, …

Exhaustive IP / Protocol Verification

VIPs



VCS

- IP & Blocks
- New Protocols
- UVM Coverage Closure

Virtual Traffic from Scalable Interfaces

Transactors

ZS5 or ZeBu EP1/2

- SoC-level
- New Protocols
- HW/SW Bring-up
- Performance &Power
- SW/HW

Rate-adapted Traffic from Real Interfaces

Speed Adaptors

ZS5, ZeBu EP1/2, HAPS-100

- HW/SW Bring-up with high fidelity
- Drivers
- Interoperability

At-speed Traffic from Real Interfaces

Protocol Interface Cards/IPK

ZeBu EP1/2 or HAPS-100

- Controller + PHY Integration
- Driver Compliance
- Protocol IP Certification
- At-Speed Interoperability Testing

Example: Arm

SW Workloads Driving Performance & Low Power Analysis

Bare-Metal

- Baremetal tests
- System Memory & cache tests
- IP/CSS scenarios

System-OS

- Operating System (Linux)
  - Real world Applications
  - Synthetic Applications/ Tests
  - Software Configurations

IP/CSS configs for baremetal testing

System Level Testbench
(ZeBu)

IP/CSS configs for OS-based testing

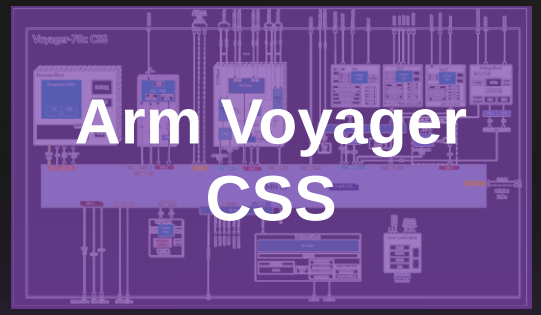
Performance analysis

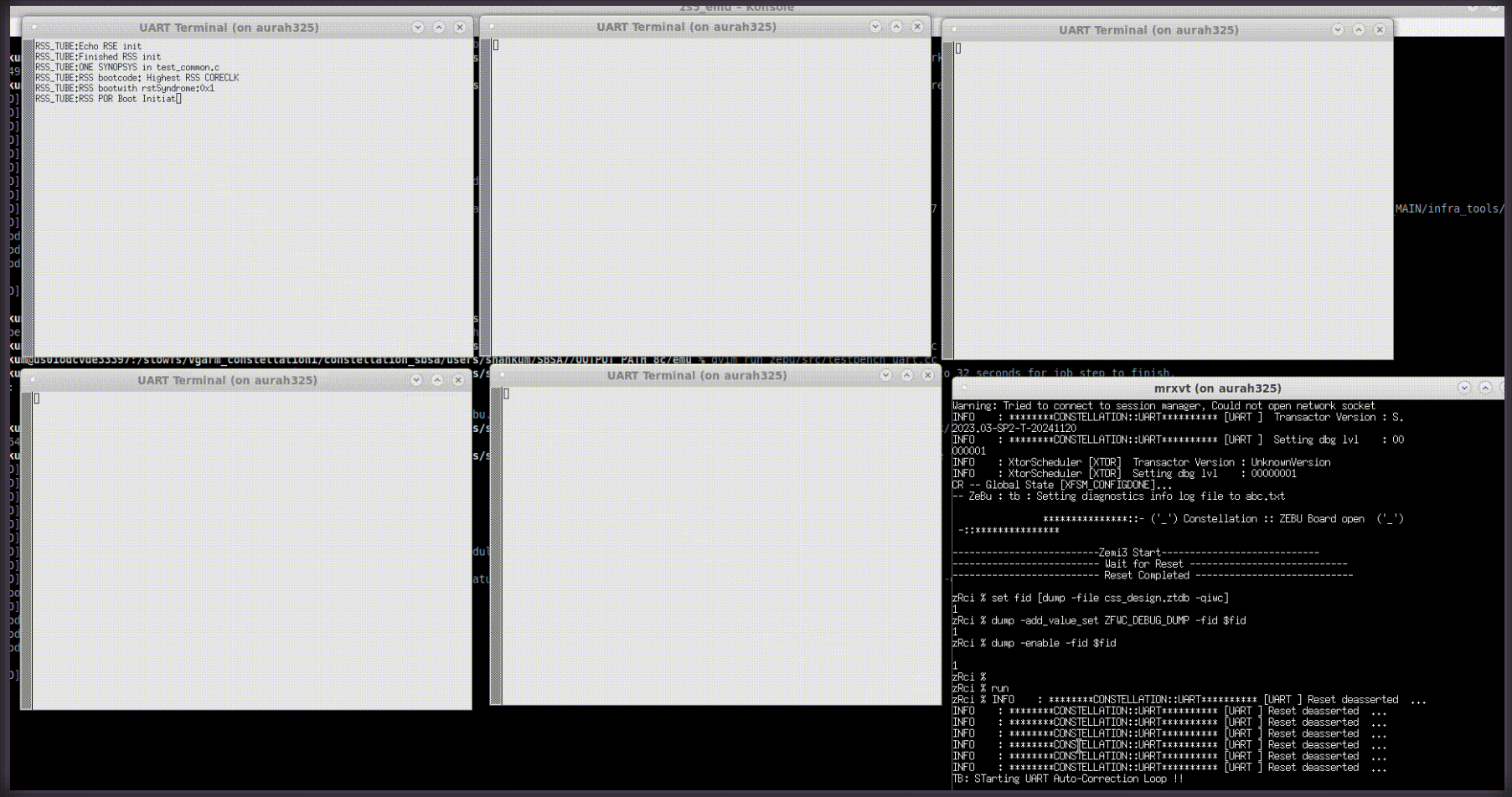
Coverage closure

Meet SW targets

Arm CSS V3 Bring-up at Synopsys

Pre-validated Arm CSS V3 Booting on ZeBu ZS5





Low Power Optimization with Real AI Workloads

Fastest Power Profiling for Real Software Workloads

Key Benefits

Large designs, Realistic workloads,
Multiple iterations per day

Actionable power profiling for
dynamic and leakage power

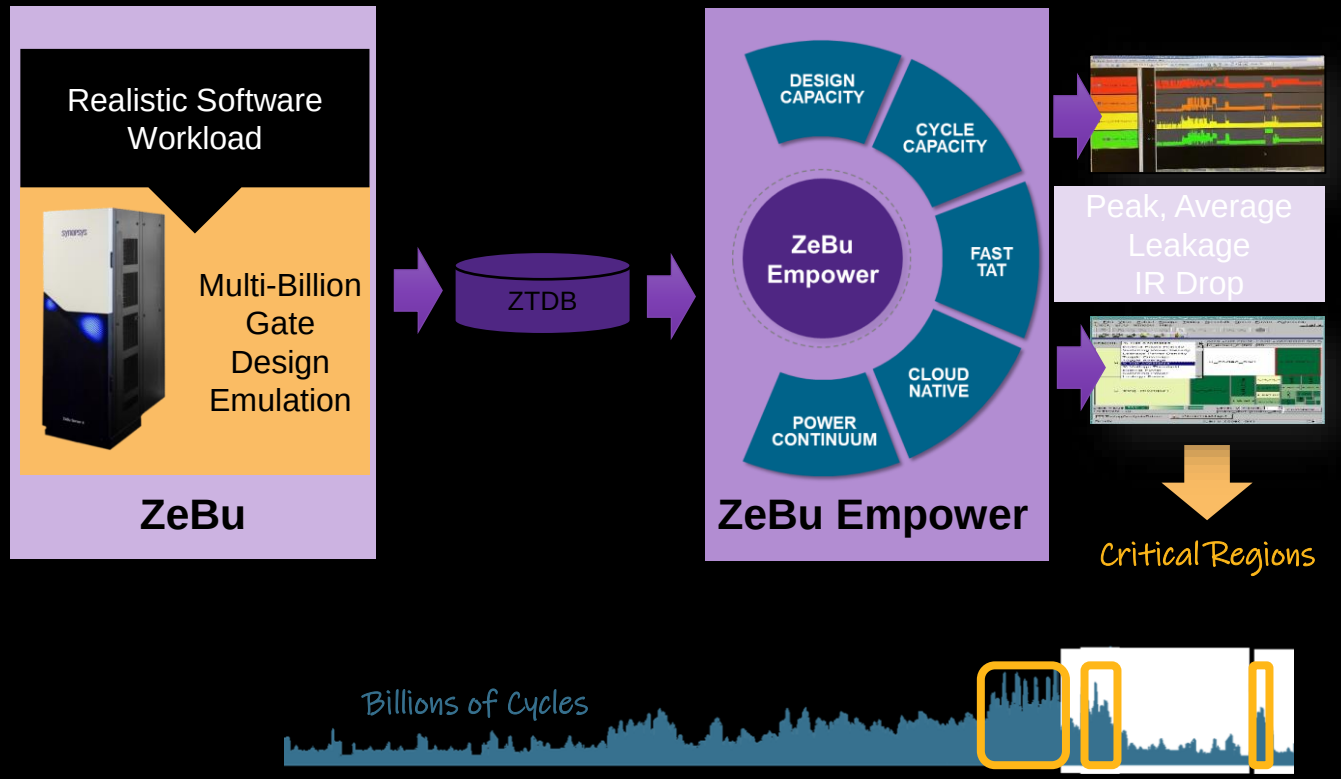
Power critical blocks and vectors
feeding into signoff analysis

"ZeBu Empower's impressive performance provides our design teams with a global perspective on power, leading them to the key areas for optimization."

Krishna Rangasayee
Founder and CEO

SiMa.ai

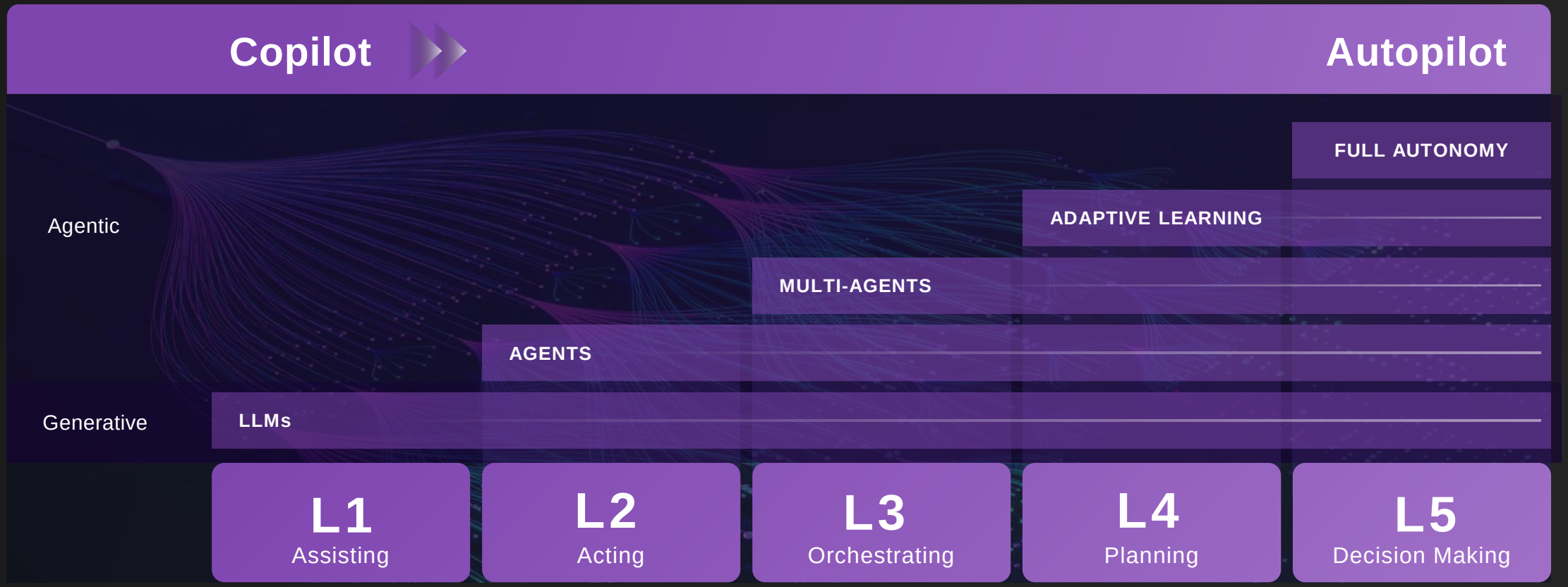
Power Emulation



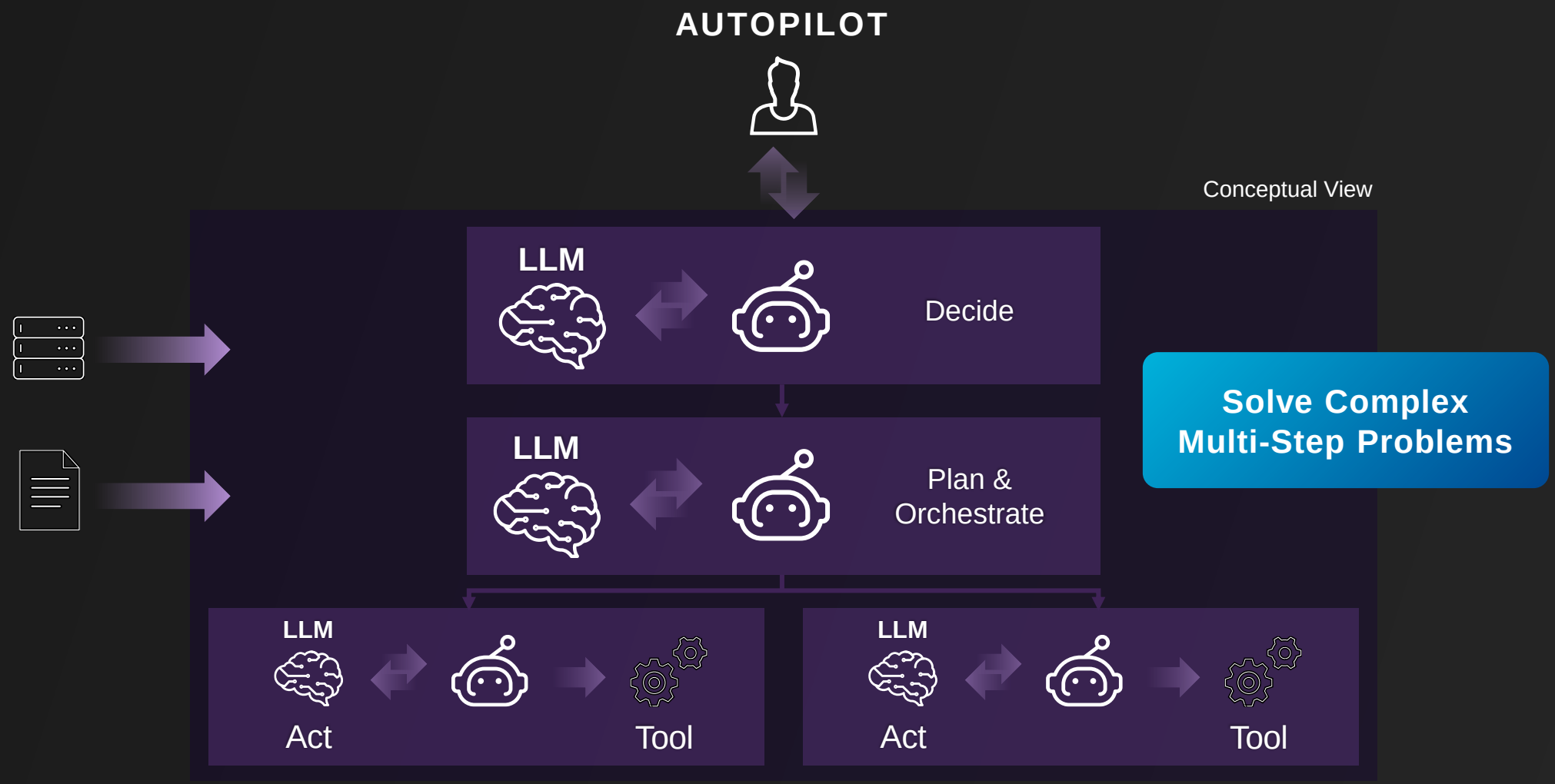
Hardware and Software Architected for Maximum Compute Throughput

AI For Productivity Improvements

Vision: AI Powered Engineering Workflows

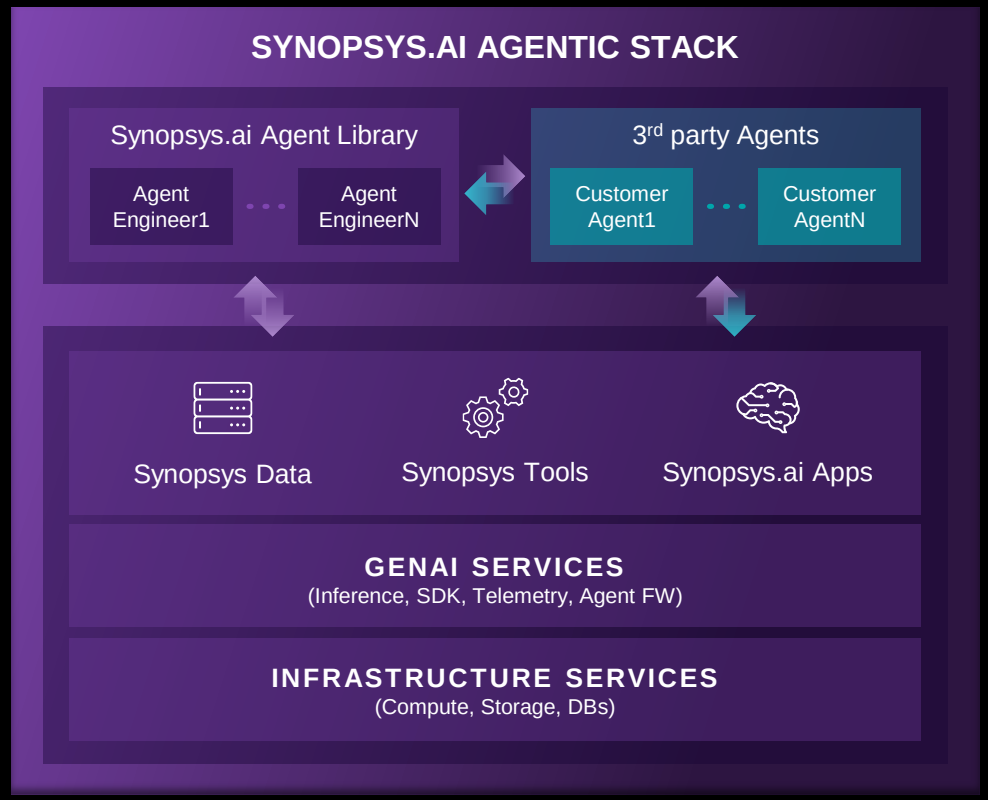


Vision: AI Powered Engineering Workflows



SNPS – MSFT Joint Partnership

Transforming engineering innovation into business success, together.



Microsoft Discovery Platform

Science Copilot

Scientific AI assistant that orchestrates specialized agents to reason over data as well as to develop and run full computational plans

Copilot as the common Platform UX
Agentic Framework
Multi-party collaboration & M365 Integration

Science Supercomputer

Infrastructure for computational plans execution

HPC as a Service
Managed Workflows
AI Model Hosting & Inference Security & Isolation

Science Bookshelf

Data layer used by Copilot for source knowledge and reasoning

Curated Knowledge Bases (Public, Paywalled, Proprietary)
Discovery Engine

Science Catalog

Set of models, tools and agents for building and running computational plans

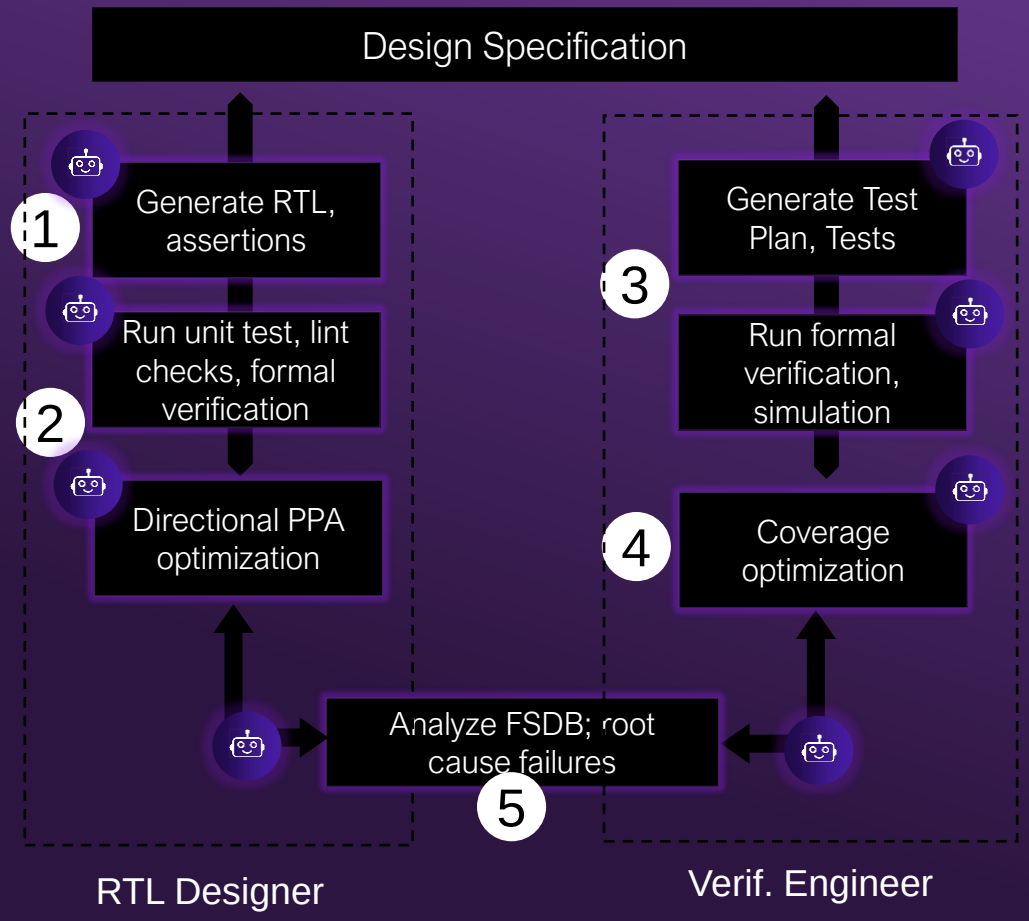
AI/ML models
Custom Agents
Computational & Visualization tools

Extensibility

Customer tools, models, and knowledge bases

BYO tools & models Marketplace

Synopsys.ai: AI Optimization and Assistants for Design and Verification



AI Apps for Verif HVPs

RTL Assistant

1. Code Advisor
2. Lint Advisor, Formal Advisor, PPA Advisor, Unit Test

Verif. Assistant

3. Spec2Testplan*, Spec2TB*, Formal Advisor
4. VSO.ai (ML)

Debug Assistant

5. Verdi Assistant, RDA (ML)

* - WIP

Outlook: Where do we go from here?

Re-engineering intelligent systems

AI model development
LLM training & inference, reasoning models

Software development
OS, middleware, application, web

Silicon development
providing required performance with lowest power usage

Fluids
airflow

Mechanical design
stress forces, interconnect

Thermal design
heating/cooling

Electrical design
reliability, PCB, power supply efficiency

Image credit: NVIDIA

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Thank you